## MB91625 Series

- Harvard architecture allowing program access and data access to be executed simultaneously
- Instruction prefetch function has been added with 4 word instruction queue of CPU
- Instruction compatible with FR family CPU
- Additional bit search instructions
- No resource instructions and coprocessor instructions
- Maximum operating frequency
- CPU : 60 MHz
- Resources : 40 MHz
- DMA controller (DMAC)
- 8 channels
- Address space : 32 bits (4 Gbytes)
- Transfer modes : Block transfer/burst transfer/demand transfer
- Address update : Increment/decrement/fixed (increment/decrement step size of 1, 2, or 4)
- Transfer data length : Selectable from 8-bit, 16-bit, 32-bit
- Block size : 1 to 16
- Number of transfers : 1 to 65535
- Transfer requests
- Requests from software
- Interrupt requests from peripheral resources (interrupt requests are shared, including external interrupts)
- Reload functions : Reload can be specified on all channels
- Priority order : Fixed (ch. $0>$ ch. $1>$ ch. $2>$ ch. $3>\ldots$...) or round-robin
- Interrupt requests : Interrupts can be generated for transfer complete, transfer error, and transfer interrupted.
- Multifunction serial interface
- 4 channels with 16-byte FIFO, 8 channels without FIFO
- Operation mode is selectable from the followings for each channel (For ch.0, ${ }^{2} \mathrm{C}$ is not available.)
- UART
- Full-duplex double buffer
- Selectable parity on/off
- Built-in dedicated baud rate generator
- External clock can be used as a serial clock
- Error detection function for parity, frame and overrun errors
- CSIO
- Full-duplex double buffer
- Built-in dedicated baud rate generator
- Overrun error detection function
- ${ }^{2} \mathrm{C}$
- Supports both standard mode (Max 100 kbps )and Fast mode (Max 400 kbps )
- Some channels are 5 V tolerant


## - Interrupts

- Total of 32 external interrupts (some pins are 5 V tolerant)
- Interrupts from peripheral resources
- Programmable interrupt levels (16 levels)
- Can be used to return from stop mode, sleep mode


## MB91625 Series

(Continued)

- Clock generation
- Main clock (MCLK) oscillator
- Sub clock (SBCLK) oscillator
- PLL clock (PLLCLK) oscillator
- Low-power dissipation mode
- Stop mode
- Watch mode
- Sleep mode
- Doze mode
- Clock division function
- Other features
- I/O port
- INIT pin is provided as a reset pin
- Watchdog timer reset, software reset
- Delay interrupt
- Power supply : Single power supply (2.7 V to 3.6 V)


## MB91625 Series

| Pin no. | Pin name | I/O circuit type ${ }^{* 1}$ | Function | CMOS level input | CMOS level hysteresis input |
| :---: | :---: | :---: | :---: | :---: | :---: |
| LQFP-100 |  |  |  |  |  |
| 8 | P34 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOA14 |  | Base timer ch. 14 TIOA pin | - | - |
|  | $\begin{aligned} & \text { SOUT7 } \\ & \text { (SDA7) } \end{aligned}$ |  | Multifunction serial interface ch. 7 output pin. This pin operates as SOUT7 when it is used in a UART/CSIO (operation modes 0 to 2 ) and as SDA7 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | OUT4 |  | 32-bit output compare ch. 4 output pin | - | - |
|  | INT12 |  | External interrupt request 12 input pin | - | $\bigcirc$ |
| 9 | P35 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOB14 |  | Base timer ch. 14 TIOB pin | - | $\bigcirc$ |
|  | SIN7 |  | Multifunction serial interface ch. 7 input pin | - | $\bigcirc$ |
|  | OUT5 |  | 32-bit output compare ch. 5 output pin | - | - |
|  | INT13 |  | External interrupt request 13 input pin | - | $\bigcirc$ |
| 10 | P36 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOA15 |  | Base timer ch. 15 TIOA pin | - | $\bigcirc$ |
|  | $\begin{aligned} & \text { SCK7 } \\ & \text { (SCL7) } \end{aligned}$ |  | Multifunction serial interface ch. 7 clock I/O pin. This pin operates as SCK7 when it is used in a UART/ CSIO (operation modes 0 to 2 ) and as SCL7 when it is used in an I2C (operation mode 4). | - | $\bigcirc$ |
|  | OUT6 |  | 32 -bit output compare ch. 6 output pin | - | - |
|  | INT14 |  | External interrupt request 14 input pin | - | $\bigcirc$ |
| 11 | P37 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOB15 |  | Base timer ch. 15 TIOB pin | - | $\bigcirc$ |
|  | OUT7 |  | 32-bit output compare ch. 7 output pin | - | - |
|  | INT15 |  | External interrupt request 15 input pin | - | $\bigcirc$ |
| 12 | P40 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | SOUT8 (SDA8) |  | Multifunction serial interface ch. 8 output pin. This pin operates as SOUT8 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA8 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |

(Continued)

## MB91625 Series

| Pin no. | Pin name | I/O circuit type*1 | Function | CMOS level input | CMOSlevelhysteresisinput |
| :---: | :---: | :---: | :---: | :---: | :---: |
| LQFP-100 |  |  |  |  |  |
| 13 | P41 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | SIN8 |  | Multifunction serial interface ch. 8 input pin | - | $\bigcirc$ |
| 14 | P42 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | $\begin{gathered} \text { SCK8 } \\ \text { (SCL8) } \end{gathered}$ |  | Multifunction serial interface ch. 8 clock I/O pin. <br> This pin operates as SCK8 when it is used in a UART/ CSIO (operation modes 0 to 2 ) and as SCL8 when it is used in an I2C (operation mode 4). | - | $\bigcirc$ |
| 15 | P43 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | P44 |  | General-purpose I/O port | - | $\bigcirc$ |
| 16 | $\begin{aligned} & \text { SOUT9 } \\ & \text { (SDA9) } \end{aligned}$ | D*2 | Multifunction serial interface ch. 9 output pin. This pin operates as SOUT9 when it is used in a UART/CSIO (operation modes 0 to 2 ) and as SDA9 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
| 17 | P45 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | SIN9 |  | Multifunction serial interface ch. 9 input pin | - | $\bigcirc$ |
|  | P46 |  | General-purpose I/O port | - | $\bigcirc$ |
| 18 | $\begin{gathered} \text { SCK9 } \\ \text { (SCL9) } \end{gathered}$ |  | Multifunction serial interface ch. 9 clock I/O pin. This pin operates as SCK9 when it is used in a UART/ CSIO (operation modes 0 to 2 ) and as SCL9 when it is used in an I2C (operation mode 4). | - | $\bigcirc$ |
| 19 | P47 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
| 20 | $\overline{\text { INIT }}$ | P | External reset input pin. A reset is valid when $\overline{\mathrm{NIT}}=\mathrm{L}$. The I/O circuit type for the Flash memory products is P. | - | $\bigcirc$ |
| 21 | MDO | P | Mode 0 pin. <br> The I/O circuit type for the Flash memory products is P. <br> During normal operation, MDO $=\mathrm{L}$ must be input. During serial programming to Flash memory, MD0 $=\mathrm{H}$ must be input. | - | $\bigcirc$ |
| 22 | MD1 | P | Mode 1 pin. Input must always be at the "L" level. The I/O circuit type for the Flash memory products is P. | - | $\bigcirc$ |
| 23 | X0 | A | Main clock (oscillation) input pin | - | $\bigcirc$ |
| 24 | X1 | A | Main clock (oscillation) I/O pin | - | - |
| 25 | Vss | - | GND pin | - | - |

(Continued)

## MB91625 Series

| Pin no. <br> LQFP-100 | Pin name | I/O circuit type ${ }^{\star 1}$ | Function | CMOS level input | CMOS level hysteresis input |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 34 | P75 | E | General-purpose I/O port | - | $\bigcirc$ |
|  | AN5 |  | 10-bit A/D converter ch. 5 analog input pin | - | - |
|  | SOUT0 |  | Multifunction serial interface ch. 0 output pin. This pin operates as SOUT0 when it is used in a UART/CSIO (operation modes 0 to 2 ). | - | - |
|  | TMIO |  | 16-bit reload timer ch. 0 input pin | - | $\bigcirc$ |
|  | OUT5_1 |  | 32-bit output compare ch. 5 output pin (Port 1) | - | - |
|  | INT21 |  | External interrupt request 21 input pin | - | $\bigcirc$ |
| 35 | P76 | E | General-purpose I/O port | - | $\bigcirc$ |
|  | AN6 |  | 10-bit A/D converter ch. 6 analog input pin | - | - |
|  | SIN0 |  | Multifunction serial interface ch. 0 input pin | - | $\bigcirc$ |
|  | TMI1 |  | 16-bit reload timer ch. 1 input pin | - | $\bigcirc$ |
|  | OUT6_1 |  | 32-bit output compare ch. 6 output pin (Port 1) | - | - |
|  | INT22 |  | External interrupt request 22 input pin | - | $\bigcirc$ |
| 36 | P77 | E | General-purpose I/O port | - | $\bigcirc$ |
|  | AN7 |  | 10-bit A/D converter ch. 7 analog input pin | - | - |
|  | SCK0 |  | Multifunction serial interface ch. 0 clock I/O pin. This pin operates as SCK0 when it is used in a UART/ CSIO (operation modes 0 to 2). | - | $\bigcirc$ |
|  | TMI2 |  | 16-bit reload timer ch. 2 input pin | - | $\bigcirc$ |
|  | OUT7_1 |  | 32-bit output compare ch. 7 output pin (Port 1) | - | - |
|  | INT23 |  | External interrupt request 23 input pin | - | $\bigcirc$ |
| 37 | P80 | E | General-purpose I/O port | - | $\bigcirc$ |
|  | AN8 |  | 10-bit A/D converter ch. 8 analog input pin | - | - |
|  | INO_1 |  | 32-bit input capture ch. 0 input pin (Port 1) | - | $\bigcirc$ |
|  | INT24 |  | External interrupt request 24 input pin | - | $\bigcirc$ |

(Continued)

## MB91625 Series

| Pin no. <br> LQFP-100 | Pin name | I/O circuit type*1 | Function | CMOS level input | CMOS level hysteresis input |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 38 | P81 | E | General-purpose I/O port | - | $\bigcirc$ |
|  | AN9 |  | 10-bit A/D converter ch. 9 analog input pin | - | - |
|  | IN1_1 |  | 32-bit input capture ch. 1 input pin (Port 1) | - | $\bigcirc$ |
|  | INT25 |  | External interrupt request 25 input pin | - | $\bigcirc$ |
| 39 | P82 | E | General-purpose I/O port | - | $\bigcirc$ |
|  | AN10 |  | 10-bit A/D converter ch. 10 analog input pin | - | - |
|  | IN2_1 |  | 32-bit input capture ch. 2 input pin (Port 1) | - | $\bigcirc$ |
|  | INT26 |  | External interrupt request 26 input pin | - | $\bigcirc$ |
| 40 | P83 | E | General-purpose I/O port | - | $\bigcirc$ |
|  | AN11 |  | 10-bit A/D converter ch. 11 analog input pin | - | - |
|  | IN3_1 |  | 32-bit input capture ch. 3 input pin (Port 1) | - | $\bigcirc$ |
|  | INT27 |  | External interrupt request 27 input pin | - | $\bigcirc$ |
| 41 | P84 | E | General-purpose I/O port | - | $\bigcirc$ |
|  | AN12 |  | 10-bit A/D converter ch. 12 analog input pin | - | - |
|  | IN4_1 |  | 32-bit input capture ch. 4 input pin (Port 1) | - | $\bigcirc$ |
|  | INT28 |  | External interrupt request 28 input pin | - | $\bigcirc$ |
| 42 | P85 | E | General-purpose I/O port | - | $\bigcirc$ |
|  | AN13 |  | 10-bit A/D converter ch. 13 analog input pin | - | - |
|  | IN5_1 |  | 32-bit input capture ch. 5 input pin (Port 1) | - | $\bigcirc$ |
|  | INT29 |  | External interrupt request 29 input pin | - | $\bigcirc$ |
| 43 | P86 | E | General-purpose I/O port | - | $\bigcirc$ |
|  | AN14 |  | 10-bit A/D converter ch. 14 analog input pin | - | - |
|  | IN6_1 |  | 32-bit input capture ch. 6 input pin (Port 1) | - | $\bigcirc$ |
|  | INT30 |  | External interrupt request 30 input pin | - | $\bigcirc$ |
| 44 | P87 | E | General-purpose I/O port | - | $\bigcirc$ |
|  | AN15 |  | 10-bit A/D converter ch. 15 analog input pin | - | - |
|  | IN7_1 |  | 32-bit input capture ch. 7 input pin (Port 1) | - | $\bigcirc$ |
|  | INT31 |  | External interrupt request 31 input pin | - | $\bigcirc$ |
| 45 | AVcc | - | 10-bit A/D converter and 8-bit D/A converter analog power pin | - | - |
| 46 | AVRH | - | 10-bit A/D converter analog reference voltage input pin | - | - |
| 47 | AVss | - | 10-bit A/D converter and 8-bit D/A converter GND pin | - | - |

(Continued)

## MB91625 Series

| Pin no. | Pin name | I/O circuit type*1 | Function | CMOS level input | CMOS level hysteresis input |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 61 | P50 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | SOUT10 <br> (SDA10) |  | Multifunction serial interface ch. 10 output pin. This pin operates as SOUT10 when it is used in a UART/CSIO (operation modes 0 to 2 ) and as SDA10 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | AINO_1 |  | Up/Down counter ch. 0 AIN input pin (Port 1) | - | $\bigcirc$ |
| 62 | P51 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | SIN10 |  | Multifunction serial interface ch. 10 input pin | - | $\bigcirc$ |
|  | BINO_1 |  | Up/Down counter ch. 0 BIN input pin (Port 1) | - | $\bigcirc$ |
| 63 | P52 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | $\begin{aligned} & \text { SCK10 } \\ & \text { (SCL10) } \end{aligned}$ |  | Multifunction serial interface ch. 10 clock I/O pin. This pin operates as SCK10 when it is used in a UART/ CSIO (operation modes 0 to 2 ) and as SCL10 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | ZIN0_1 |  | Up/Down counter ch. 0 ZIN input pin (Port 1) | - | $\bigcirc$ |
| 64 | P53 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | FRCK1 |  | 32-bit free-run timer ch. 1 external clock input pin | - | $\bigcirc$ |
|  | INT21_2 |  | External interrupt request 21 input pin (Port 2) | - | $\bigcirc$ |
| 65 | P54 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | SOUT11 <br> (SDA11) |  | Multifunction serial interface ch. 11 output pin. This pin operates as SOUT11 when it is used in a UART/CSIO (operation modes 0 to 2 ) and as SDA11 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | AlN1_1 |  | Up/Down counter ch. 1 AIN input pin (Port 1) | - | $\bigcirc$ |
| 66 | P55 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | SIN11 |  | Multifunction serial interface ch. 11 input pin | - | $\bigcirc$ |
|  | BIN1_1 |  | Up/Down counter ch. 1 BIN input pin (Port 1) | - | $\bigcirc$ |
|  | ADTRG0 |  | 10-bit A/D converter external trigger input pin | - | $\bigcirc$ |

(Continued)

## MB91625 Series

| Pin no. | Pin name | I/O circuit type*1 | Function | CMOS level input | CMOS level hysteresis input |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 67 | P56 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | SCK11 <br> (SCL11) |  | Multifunction serial interface ch. 11 clock I/O pin. This pin operates as SCK11 when it is used in a UART/ CSIO (operation modes 0 to 2 ) and as SCL11 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | ZIN1_1 |  | Up/Down counter ch. 1 ZIN input pin (Port 1) | - | $\bigcirc$ |
|  | FRCK0 |  | 32-bit free-run timer ch. 0 external clock input pin | - | $\bigcirc$ |
| 68 | P57 | C | General-purpose I/O port | - | $\bigcirc$ |
| 69 | P60 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | AIN2_1 |  | Up/Down counter ch. 2 AIN input pin (Port 1) | - | $\bigcirc$ |
| 70 | P61 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | BIN2_1 |  | Up/Down counter ch. 2 BIN input pin (Port 1) | - | $\bigcirc$ |
| 71 | P62 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | ZIN2_1 |  | Up/Down counter ch. 2 ZIN input pin (Port 1) | - | $\bigcirc$ |
| 72 | P63 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | FRCK1_1 |  | 32-bit free-run timer ch. 1 external clock input pin (Port 1) | - | $\bigcirc$ |
|  | INT22_2 |  | External interrupt request 22 input pin (Port 2) | - | $\bigcirc$ |
| 73 | P64 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | AlN3_1 |  | Up/Down counter ch. 3 AIN input pin (Port 1) | - | $\bigcirc$ |
| 74 | P65 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | BIN3_1 |  | Up/Down counter ch. 3 BIN input pin (Port 1) | - | $\bigcirc$ |
|  | $\begin{gathered} \text { ADTRGO } \\ 1 \end{gathered}$ |  | 10-bit A/D converter external trigger input pin (Port 1) | - | $\bigcirc$ |
| 75 | P66 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | ZIN3_1 |  | Up/Down counter ch. 3 ZIN input pin (Port 1) | - | $\bigcirc$ |
|  | FRCK0_1 |  | 32-bit free-run timer ch. 0 external clock input pin (Port 1) | - | $\bigcirc$ |
| 76 | P67 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | INT23_2 |  | External interrupt request 23 input pin (Port 2) | - | $\bigcirc$ |

(Continued)

## MB91625 Series

| Prin no. | Pin name | I/O circuit type*1 | Function | CMOS level input | CMOS level hysteresis input |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 83 | P06 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOA3 |  | Base timer ch. 3 TIOA pin | - | $\bigcirc$ |
|  | $\begin{aligned} & \text { SCK1 } \\ & \text { (SCL1) } \end{aligned}$ |  | Multifunction serial interface ch. 1 clock I/O pin. This pin operates as SCK1 when it is used in a UART/ CSIO (operation modes 0 to 2 ) and as SCL1 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | IN6 |  | 32-bit input capture ch. 6 input pin | - | $\bigcirc$ |
| 84 | P07 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOB3 |  | Base timer ch. 3 TIOB pin | - | $\bigcirc$ |
|  | IN7 |  | 32 -bit input capture ch. 7 input pin | - | $\bigcirc$ |
| 85 | P10 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOA4 |  | Base timer ch. 4 TIOA pin | - | - |
|  | $\begin{aligned} & \text { SOUT2 } \\ & \text { (SDA2) } \end{aligned}$ |  | Multifunction serial interface ch. 2 output pin. This pin operates as SOUT2 when it is used in a UART/CSIO (operation modes 0 to 2 ) and as SDA2 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | AINO |  | Up/Down counter ch. 0 AIN input pin | - | $\bigcirc$ |
|  | INTO |  | External interrupt request 0 input pin | - | $\bigcirc$ |
| 86 | P11 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOB4 |  | Base timer ch. 4 TIOB pin | - | $\bigcirc$ |
|  | SIN2 |  | Multifunction serial interface ch. 2 input pin | - | $\bigcirc$ |
|  | BIN0 |  | Up/Down counter ch.0 BIN input pin | - | $\bigcirc$ |
|  | INT1 |  | External interrupt request 1 input pin | - | $\bigcirc$ |
| 87 | P12 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOA5 |  | Base timer ch. 5 TIOA pin | - | $\bigcirc$ |
|  | $\begin{gathered} \text { SCK2 } \\ \text { (SCL2) } \end{gathered}$ |  | Multifunction serial interface ch. 2 clock I/O pin. This pin operates as SCK2 when it is used in a UART/ CSIO (operation modes 0 to 2 ) and as SCL2 when it is used in an ${ }^{12} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | ZIN0 |  | Up/Down counter ch. 0 ZIN input pin | - | $\bigcirc$ |
|  | INT2 |  | External interrupt request 2 input pin | - | $\bigcirc$ |
| 88 | P13 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOB5 |  | Base timer ch. 5 TIOB pin | - | $\bigcirc$ |
|  | INT3 |  | External interrupt request 3 input pin | - | $\bigcirc$ |

(Continued)

## MB91625 Series

| Pin no. | Pin name | I/O circuit type*1 | Function | CMOS level input | CMOS level hysteresis input |
| :---: | :---: | :---: | :---: | :---: | :---: |
| LQFP-100 |  |  |  |  |  |
| 89 | P14 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOA6 |  | Base timer ch. 6 TIOA pin | - | - |
|  | $\begin{aligned} & \text { SOUT3 } \\ & \text { (SDA3) } \end{aligned}$ |  | Multifunction serial interface ch. 3 output pin. This pin operates as SOUT3 when the product is used in a UART/CSIO (operation modes 0 to 2 ) and as SDA3 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | AIN1 |  | Up/Down counter ch. 1 AIN input pin | - | $\bigcirc$ |
|  | INT4 |  | External interrupt request 4 input pin | - | $\bigcirc$ |
| 90 | P15 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOB6 |  | Base timer ch. 6 TIOB pin | - | $\bigcirc$ |
|  | SIN3 |  | Multifunction serial interface ch. 3 input pin | - | $\bigcirc$ |
|  | BIN1 |  | Up/Down counter ch. 1 BIN input pin | - | $\bigcirc$ |
|  | INT5 |  | External interrupt request 5 input pin | - | $\bigcirc$ |
| 91 | P16 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOA7 |  | Base timer ch. 7 TIOA pin | - | $\bigcirc$ |
|  | $\begin{aligned} & \text { SCK3 } \\ & \text { (SCL3) } \end{aligned}$ |  | Multifunction serial interface ch. 3 clock I/O pin. This pin operates as SCK3 when it is used in a UART/ CSIO (operation modes 0 to 2) and as SCL3 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | ZIN1 |  | Up/Down counter ch. 1 ZIN input pin | - | $\bigcirc$ |
|  | INT6 |  | External interrupt request 6 input pin | - | $\bigcirc$ |
| 92 | P17 | C | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOB7 |  | Base timer ch. 7 TIOB pin | - | $\bigcirc$ |
|  | INT7 |  | External interrupt request 7 input pin | - | $\bigcirc$ |
| 93 | P20 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOA8 |  | Base timer ch. 8 TIOA pin | - | - |
|  | SOUT4 (SDA4) |  | Multifunction serial interface ch. 4 output pin. This pin operates as SOUT4 when it is used in a UART/CSIO (operation modes 0 to 2) and as SDA4 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | AIN2 |  | Up/Down counter ch. 2 AIN input pin | - | $\bigcirc$ |
| 94 | P21 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOB8 |  | Base timer ch. 8 TIOB pin | - | $\bigcirc$ |
|  | SIN4 |  | Multifunction serial interface ch. 4 input pin | - | $\bigcirc$ |
|  | BIN2 |  | Up/Down counter ch. 2 BIN input pin | - | $\bigcirc$ |

(Continued)

## MB91625 Series

(Continued)

| Pin no. | Pin name | $\begin{gathered} \text { I/O } \\ \text { circuit } \\ \text { type } \end{gathered}$ | Function | CMOS level input | CMOS level hysteresis input |
| :---: | :---: | :---: | :---: | :---: | :---: |
| 95 | P22 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOA9 |  | Base timer ch. 9 TIOA pin | - | $\bigcirc$ |
|  | $\begin{gathered} \text { SCK4 } \\ \text { (SCL4) } \end{gathered}$ |  | Multifunction serial interface ch. 4 clock I/O pin. This pin operates as SCK4 when it is used in a UART/ CSIO (operation modes 0 to 2 ) and as SCL4 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | ZIN2 |  | Up/Down counter ch. 2 ZIN input pin | - | $\bigcirc$ |
| 96 | P23 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOB9 |  | Base timer ch. 9 TIOB pin | - | $\bigcirc$ |
| 97 | P24 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOA10 |  | Base timer ch. 10 TIOA pin | - | - |
|  | $\begin{aligned} & \text { SOUT5 } \\ & \text { (SDA5) } \end{aligned}$ |  | Multifunction serial interface ch. 5 output pin. This pin operates as SOUT5 when it is used in a UART/CSIO (operation modes 0 to 2 ) and as SDA5 when it is used in an $I^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | AIN3 |  | Up/Down counter ch. 3 AIN input pin | - | $\bigcirc$ |
|  | OUTO |  | 32-bit output compare ch. 0 output pin | - | - |
| 98 | P25 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOB10 |  | Base timer ch. 10 TIOB pin | - | $\bigcirc$ |
|  | SIN5 |  | Multifunction serial interface ch. 5 input pin | - | $\bigcirc$ |
|  | BIN3 |  | Up/Down counter ch. 3 BIN input pin | - | $\bigcirc$ |
|  | OUT1 |  | 32-bit output compare ch. 1 output pin | - | - |
| 99 | P26 | D*2 | General-purpose I/O port | - | $\bigcirc$ |
|  | TIOA11 |  | Base timer ch. 11 TIOA pin | - | $\bigcirc$ |
|  | $\begin{aligned} & \text { SCK5 } \\ & \text { (SCL5) } \end{aligned}$ |  | Multifunction serial interface ch. 5 clock I/O pin. This pin operates as SCK5 when it is used in a UART/ CSIO (operation modes 0 to 2 ) and as SCL5 when it is used in an ${ }^{2} \mathrm{C}$ (operation mode 4). | - | $\bigcirc$ |
|  | ZIN3 |  | Up/Down counter ch. 3 ZIN input pin | - | $\bigcirc$ |
|  | OUT2 |  | 32-bit output compare ch. 2 output pin | - | - |
| 100 | Vcc | - | Power pin | - | - |

*1: Refer to "■ I/O CIRCUIT TYPE" for details on the I/O circuit types.
*2: 5 V tolerant pin

## MB91625 Series

| Type | Circuit | Remarks |
| :---: | :---: | :---: |
| D |  | - CMOS level output <br> - CMOS level hysteresis input <br> - 5 V tolerant input <br> - With standby control <br> Note: When this pin is used as an $I^{2} \mathrm{C}$ pin, the digital output P -ch transistor is always off. |
| E |  | - CMOS level output <br> - CMOS level hysteresis input <br> - With input control <br> - Analog input <br> - With pull-up control <br> - With standby control |

(Continued)

## MB91625 Series


(Continued)

## MB91625 Series

(Continued)

| Type | Circuit | Remarks |
| :---: | :---: | :---: |
| P |  | - Flash memory product only <br> - CMOS level hysteresis input <br> - High voltage control for testing Flash memory |

## MB91625 Series

## PRECAUTIONS FOR HANDLING THE DEVICES

Any semiconductor devices have inherently a certain rate of failure. The possibility of failure is greatly affected by the conditions in which they are used (circuit conditions, environmental conditions, etc.). This page describes precautions that must be observed to minimize the chance of failure and to obtain higher reliability from your FUJITSU MICROELECTRONICS semiconductor devices.

## 1. Precautions for Product Design

This section describes precautions when designing electronic equipment using semiconductor devices.

- Absolute Maximum Ratings

Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

## - Recommended Operating Conditions

The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## - Processing and Protection of Pins

These precautions must be followed when handling the pins which connect semiconductor devices to power supply and input/output functions.
(1) Preventing Over-Voltage and Over-Current Conditions

Exposure to voltage or current levels in excess of maximum ratings at any pin is likely to cause deterioration within the device, and in extreme cases leads to permanent damage of the device. Try to prevent such overvoltage or over-current conditions at the design stage.
(2) Protection of Output Pins

Shorting of output pins to supply pins or other output pins, or connection to large capacitance can cause large current flows. Such conditions if present for extended periods of time can damage the device.
Therefore, avoid this type of connection.
(3) Handling of Unused Input Pins

Unconnected input pins with very high impedance levels can adversely affect stability of operation. Such pins should be connected through an appropriate resistance to a power supply pin or ground pin.

## MB91625 Series

- Baking

Packages that have absorbed moisture may be de-moisturized by baking (heat drying). Follow the FUJITSU MICROELECTRONICS recommended conditions for baking.
Condition: $+125^{\circ} \mathrm{C} / 24 \mathrm{~h}$

- Static Electricity

Because semiconductor devices are particularly susceptible to damage by static electricity, you must take the following precautions:
(a) Maintain relative humidity in the working environment between $40 \%$ and $70 \%$. Use of an apparatus for ion generation may be needed to remove electricity.
(b) Electrically ground all conveyors, solder vessels, soldering irons and peripheral equipment.
(c) Eliminate static body electricity by the use of rings or bracelets connected to ground through high resistance (on the level of $1 \mathrm{M} \Omega$ ). Wearing of conductive clothing and shoes, use of conductive floor mats and other measures to minimize shock loads is recommended.
(d) Ground all fixtures and instruments, or protect with anti-static measures.
(e) Avoid the use of styrofoam or other highly static-prone materials for storage of completed board assemblies.

## 3. Precautions for Use Environment

Reliability of semiconductor devices depends on ambient temperature and other conditions as described above. For reliable performance, do the following:
(1) Humidity

Prolonged use in high humidity can lead to leakage in devices as well as printed circuit boards. If high humidity levels are anticipated, consider anti-humidity processing.
(2) Discharge of Static Electricity

When high-voltage charges exist close to semiconductor devices, discharges can cause abnormal operation. In such cases, use anti-static measures or processing to prevent discharges.
(3) Corrosive Gases, Dust, or Oil

Exposure to corrosive gases or contact with dust or oil may lead to chemical reactions that will adversely affect the device. If you use devices in such conditions, consider ways to prevent such exposure or to protect the devices.
(4) Radiation, Including Cosmic Radiation

Most devices are not designed for environments involving exposure to radiation or cosmic radiation. Users should provide shielding as appropriate.
(5) Smoke, Flame

Note: Plastic molded devices are flammable, and therefore should not be used near combustible substances. If devices begin to smoke or burn, there is danger of the release of toxic gases.
Customers considering the use of FUJITSU MICROELECTRONICS products in other special environmental conditions should consult with sales representatives.

## MB91625 Series

## HANDLING DEVICES

- Power supply pins

In products with multiple Vcc and Vss pins, respective pins at the same potential are interconnected within the device in order to prevent malfunctions such as latch-up. However, all of these pins should be connected externally to the power supply or ground lines in order to reduce electromagnetic emission levels, to prevent abnormal operation of strobe signals caused by the rise in the ground level, and to conform to the total output current rating. Moreover, connect the current supply source with the $\mathrm{V}_{\mathrm{cc}}$ and $\mathrm{V}_{\mathrm{ss}}$ pins of this device at low impedance.
It is also advisable that a ceramic capacitor of approximately $0.1 \mu \mathrm{~F}$ be connected as a bypass capacitor between $V_{c c}$ and $V_{s s}$ pins near this device.

- Crystal oscillator circuit

Noise near the X 0 and X 1 pins may cause the device to malfunction. Design the printed circuit board so that XO , X1, the crystal oscillator (or ceramic oscillator), and the bypass capacitor to ground are located as close to the device as possible.
It is strongly recommended that the PC board artwork be designed such that the X 0 and X 1 pins are surrounded by ground plane as this is expected to produce stable operation.
If a 32 kHz oscillator is used (X0A, X1A), use the PK2 pin for an input that changes as infrequently as possible. Furthermore, take steps such as shown in the following figure to prevent the XOA and PK2 wiring from running parallel to each other.
If 32 kHz oscillation is not used, there are no limitations.


- Using an external clock

When using an external clock, the clock signal should be input to the X 0 pin only and the X 1 should be kept open.

- Example of Using an External Clock MB91625 series



## MB91625 Series

- C Pin

As MB91625 series includes an internal regulator, always connect a bypass capacitor of approximately $4.7 \mu \mathrm{~F}$ to the C pin for use by the regulator.


- Mode pins (MD0, MD1)

Connect the MD pin (MD0, MD1) directly to Vcc or Vss pins. Design the printed circuit board such that the pullup/down resistance stays low, as well as the distance between the mode pins and $\mathrm{V}_{\text {cc }}$ pins or $\mathrm{V}_{\text {ss }}$ pins is as short as possible and the connection impedance is low, when the pins are pulled-up/down such as for switching the pin level and rewriting the Flash memory data. It is because of preventing the device erroneously switching to test mode due to noise.

- Notes on power-on
- To ensure that the internal regulator and the oscillator have stabilized immediately after the power is turned on, keep an "L" level input connected to the INIT pin for the duration of the regulator voltage stabilization wait time + the oscillator start time of the oscillator + the main oscillator stabilization wait time.
- Turn power on/off in the following order

Turning on: $\mathrm{Vcc} \rightarrow \mathrm{AV} \mathrm{cc} \rightarrow \mathrm{AVRH}$
Turning off: AVRH $\rightarrow \mathrm{AVcc} \rightarrow \mathrm{Vcc}$
Release the reset (INIT pin "L" level to "H" level) after the power supply has stabilized.

- Caution on Operations during PLL Clock Mode

On this microcontroller, if in case the crystal oscillator breaks off or an external reference clock input stops while the PLL clock mode is selected, a self-oscillator circuit contained in the PLL may continue its operation at its self-running frequency.
However, FUJITSU MICROELECTRONICS will not guarantee results of operations if such failure occurs.

## MB91625 Series

## BLOCK DIAGRAM



## MB91625 Series

## MEMORY SPACE

## 1. Memory Space

The FR family has 4 Gbytes of logical address space ( $2^{32}$ addresses) available to the CPU by linear access.

- Direct Addressing Areas

The following areas in the address space are used as I/O areas.
These areas are called direct addressing areas, and the address of an operand in these areas can be specified directly within an instruction. The size of the directly addressable area depends on the length of the data being accessed as follows.

- Byte data access : 0000 0000н to 0000 00FFн
- Half word data access : 0000 0000н to 000001 FFн
- Word data access :0000 0000н to 000003 FF н


## MB91625 Series

## 2. Memory Map



Notes: • Small sector area is related to flash products only. Please refer to "Flash Memory" in the "Hardware Manual" for more details.

- Do not access the reserved areas.


## MB91625 Series

I/O MAP
[How to read the table]

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | + 0 | + 1 | + 2 | + 3 |  |
| 0000 0000н | PDR0 [R/W] B, H XXXXXXXX | PDR1 [R/W] B, H XXXXXXXX | PDR2 [R/W] B, H XXXXXXXXXXX | PDR3 [R/W] B, H XXXXXXXX | Port data register |
| 0000 003CH | $\begin{gathered} \hline \text { WDTCR0 [R/W] } \\ \text { B, H } \\ -0--0000 \end{gathered}$ | $\begin{gathered} \hline \text { WDTCPRO [R/W] } \\ \text { B, H } \\ 00000000 \end{gathered}$ |  |  | Watchdog timer |
| $\begin{gathered} 0000 \text { 0040H } \\ \hline \end{gathered}$ | EIRRO [R/W] B, H, W <br> 4 00010000 | $\begin{gathered} \text { ENIR0 }[R / W] \\ \text { B, H, W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { ELVRO [R/ } \\ 00000000 \end{gathered}$ | $\begin{aligned} & N] \text { B, H, W } \\ & 00000000 \end{aligned}$ | External interrupt 0 to 7 |
|  | B | Initial value after re"1": Initial value"1" 0 " : Initial value"0" X - " : Initial value unerved bitAccess unit(B : byte, H : half woRead/write attribute <br> "R" $:$ Indicates th <br> "R/W": Indicates th <br> "W" : Indicates thRegister name (colat address $4 \mathrm{n}+2 . .$. | et <br> defined or undefined bit <br> d, W : word) <br> at there is a read on at there is a read/wr at there is a write on <br> mn 1 of the register | : Reserved area <br> y bit. <br> te bit. <br> y bit. <br> is at address $4 n$, | mn 2 is |

Notes: - When performing a data access, the addresses should be as below.

- Word access : Address should be multiples of 4 (least significant 2 bits should be "008")
- Half word access : Address should be multiples of 2 (least significant bit should be " $\mathrm{O}_{\mathrm{B}}$ ")
- Byte access: -
- Do not access the reserved areas.


## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 0000н | $\begin{gathered} \hline \text { PDRO }[R / W] B, H \\ X X X X X X X \end{gathered}$ | PDR1 [R/W] B,H XXXXXXXX | PDR2 [R/W] B,H XXXXXXXX | PDR3 [R/W] B,H XXXXXXXX | Port data register |
| 0000 0004н | PDR4 [R/W] B,H XXXXXXXX | PDR5 [R/W] B,H XXXXXXXX | PDR6 [R/W] B,H XXXXXXXX | PDR7 [R/W] B,H XXXXXXXX |  |
| 0000 0008H | PDR8 [R/W] B,H $X X X X X X X X$ | $\begin{gathered} \text { PDR9 [R/W] B,H } \\ ----X X X ~ \end{gathered}$ | PDRA [R/W] B,H XXXXXXXX | - |  |
| $\begin{array}{\|c} 0000 \text { 000CH } \\ \text { to } \\ 00000010 \mathrm{H} \end{array}$ | - |  |  |  |  |
| 0000 0014 | $\underset{-----X X X ~}{\text { PDRK }}$ | - |  |  |  |
| $\begin{gathered} 0000 \text { 0018 } \\ \text { to } \\ 000001 \text { C }_{H} \end{gathered}$ | - |  |  |  |  |
| $\begin{gathered} 00000020_{\mathrm{H}} \\ \text { to } \\ 0000038 \mathrm{H} \end{gathered}$ | - |  |  |  | Reserved |
| 0000 003Cн | $\begin{gathered} \hline \text { WDTCRO }[R / W] \\ B, H \\ -0--0000 \end{gathered}$ | $\begin{gathered} \hline \text { WDTCPRO }[\mathrm{R} / \mathrm{W}] \\ \text { B,H } \\ 00000000 \end{gathered}$ | - |  | Watchdog timer |
| 0000 0040н | $\begin{gathered} \hline \text { EIRRO [R/W] } \\ B, H, W \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { ENIRO [R/W] } \\ B, H, W \\ 00000000 \end{gathered}$ | ELVRO [R/W] B,H,W 0000000000000000 |  | External interrupt 0 to 7 |
| 0000 0044 | DICR [------0 | - |  |  | Delay interrupt |
| 0000 0048 | TMRLRAO [R/W] H XXXXXXXX XXXXXXXX |  | TMR0 [R] H XXXXXXXX XXXXXXXX |  | 16-bit |
| 0000 004CH | - |  | $\begin{aligned} & \hline \text { TMCSRO [R/W] H } \\ & --000000-000000 \end{aligned}$ |  | ch. 0 |
| 0000 0050н | TMRLRA1 [R/W] H XXXXXXXX XXXXXXXX |  | TMR1 [R] H XXXXXXXX XXXXXXXX |  | $\begin{aligned} & \text { 16-bit } \\ & \text { reload timer } \\ & \text { ch. } 1 \end{aligned}$ |
| 0000 0054н | - |  | TMCSR1 [R/W] H <br> --000000 --000000 |  |  |
| 0000 0058н | TMRLRA2 [R/W] H XXXXXXXX XXXXXXXX |  | TMR2 [R] H XXXXXXXX XXXXXXXX |  | 16-bit reload timer ch. 2 |
| 0000 005CH | - |  | $\begin{aligned} & \hline \text { TMCSR2 [R/W] H } \\ & --000000--000000 \end{aligned}$ |  |  |

(Continued)

## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 0060н | $\begin{gathered} \hline \text { SCR0 } \\ {[R / W] B, H, W} \\ 0--00000 \end{gathered}$ | $\begin{gathered} \hline \text { SMR0 }[R / W] \\ B, H, W \\ 000-0000 \end{gathered}$ | $\begin{gathered} \hline \text { SSRO [R,R/W] } \\ B, H, W \\ 0-000011 \end{gathered}$ | ESCRO [R/W] B,H,W -0000000 | Multi-function |
| 0000 0064н |  |  | $\begin{gathered} \hline \text { BGR10 [R/W] } \\ H, W \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { BGR00 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ | ch. 0 |
| 0000 0068н | $\begin{gathered} \hline \text { SCR1 }[R / W] / \\ \text { IBCR1 } \\ {[R, R / W] B, H, W^{* 2}} \\ 0--00000 \end{gathered}$ | $\begin{gathered} \text { SMR1 [R/W] } \\ \text { B,H,W } \\ 000-0000 \end{gathered}$ | $\begin{gathered} \text { SSR1 [R,R/W] } \\ B, H, W \\ 0-000011 \end{gathered}$ | $\begin{gathered} \text { ESCR1 [R/W]/ } \\ \text { IBSR1 } \\ {[R, R / W] B, H, W * 2} \\ -0000000 \end{gathered}$ | Multi-function serial interface ch. 1 |
| 0000 006Сн | RDR1 [R]/ TDR1[W] B,H, ${ }^{*-----0} 00000000$ |  | $\begin{gathered} \hline \text { BGR11 [R/W] } \\ H, W \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { BGR01 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 0070н | ISMK1 [------- ${ }^{\text {- }}$ | $\begin{gathered} \text { ISBA1 [R/W] } \\ \mathrm{B}, \mathrm{H}^{* 2} \\ ------ \end{gathered}$ | - |  |  |
| 0000 0074 | $\begin{gathered} \text { SCR2 [R/W]/ } \\ \text { IBCR2 } \\ {[R, R / W] B, H, W * 2} \\ 0--00000 \end{gathered}$ | $\begin{gathered} \text { SMR2 [R/W] } \\ \text { B,H,W } \\ 000-0000 \end{gathered}$ | $\begin{gathered} \text { SSR2 [R,R/W] } \\ \text { B,H,W } \\ 0-000011 \end{gathered}$ | $\begin{gathered} \text { ESCR2 }[\mathrm{R} / \mathrm{W}] / \\ \text { IBSR2 }[\mathrm{R}, \mathrm{R} / \mathrm{W}] \\ \mathrm{B}, \mathrm{H}, \mathrm{~W}^{* 2} \\ -0000000 \end{gathered}$ | Multi-function serial interface ch. 2 |
| 0000 0078н |  |  | $\begin{gathered} \hline \text { BGR12 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { BGR02 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 007Сн | ISMK2 [R/W] B, $\mathrm{H}^{* 2}$ $\qquad$ | $\begin{gathered} \text { ISBA2 [R/W] } \\ \substack{\mathrm{B}, \mathrm{H}^{\star 2} \\ ------} \end{gathered}$ | - |  |  |
| 0000 0080н | $\begin{gathered} \hline \text { SCR3 }[R / W] / \\ \text { IBCR3 } \\ {[R, R / W] B, H, W^{* 2}} \\ 0--00000 \end{gathered}$ | $\begin{gathered} \text { SMR3 [R/W] } \\ \text { B,H,W } \\ 000-0000 \end{gathered}$ | $\begin{gathered} \text { SSR3 [R,R/W] } \\ B, H, W \\ 0-000011 \end{gathered}$ | $\begin{gathered} \text { ESCR3 }[\mathrm{R} / \mathrm{W}] / \\ \text { IBSR3 }[\mathrm{R}, \mathrm{R} / \mathrm{W}] \\ \mathrm{B}, \mathrm{H}, \mathrm{~W}^{* 2} \\ -0000000 \end{gathered}$ | Multi-function serial interface ch. 3 |
| 0000 0084н |  |  | $\begin{gathered} \text { BGR13 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { BGR03 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 0088н | ISMK3 [R/------ B, ${ }^{*}$ | $\begin{gathered} \hline \text { ISBA3 [R/W] } \\ \text { B,------- } \end{gathered}$ | - |  |  |

(Continued)

## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 008Сн | $\begin{gathered} \text { SCR4 }[R / W] / \\ \text { IBCR4 } \\ {[R, R / W] B, H, W^{* 2}} \\ 0--00000 \end{gathered}$ | $\begin{gathered} \text { SMR4 [R/W] } \\ \text { B,H,W } \\ 000-0000 \end{gathered}$ | $\begin{gathered} \text { SSR4 [R,R/W] } \\ \text { B,H,W } \\ 0-000011 \end{gathered}$ | $\begin{gathered} \text { ESCR4 }[\mathrm{R} / \mathrm{W}] / \\ \text { IBSR4 }[\mathrm{R}, \mathrm{R} / \mathrm{W}] \\ \mathrm{B}, \mathrm{H}, \mathrm{~W}^{* 2} \\ -0000000 \end{gathered}$ | Multi-function serial interface ch. 4 |
| 0000 0090н | $\begin{gathered} \text { RDR4 [R] / TDR4 [W] B,H, W** }{ }_{-----0000000} 000000 \end{gathered}$ |  | $\begin{gathered} \text { BGR14 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { BGR04 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 0094H | ISMK4 [R/W] B, $\mathrm{H}^{\star 2}$ | $\begin{gathered} \text { ISBA4 [R/W] } \\ \substack{\mathrm{B}, \mathrm{H}^{* 2} \\ ------} \end{gathered}$ | - |  |  |
| 0000 0098н | $\begin{gathered} \text { SCR5 [R/W]/ } \\ \text { IBCR5 } \\ {[R, \mathrm{R} / \mathrm{W}] \mathrm{B}, \mathrm{H}, \mathrm{~W}^{* 2}} \\ 0--00000 \end{gathered}$ | $\begin{gathered} \text { SMR5 [R/W] } \\ \text { B,H,W } \\ 000-0000 \end{gathered}$ | $\begin{gathered} \text { SSR5 [R,R/W] } \\ B, H, W \\ 0-000011 \end{gathered}$ | $\begin{gathered} \text { ESCR5 }[\mathrm{R} / \mathrm{W}] / / \\ \text { IBSR5 }[R, R / W] \\ \mathrm{B}, \mathrm{H}, \mathrm{~W}^{* 2} \\ -000000 \end{gathered}$ | Multi-function serial interface ch. 5 |
| 0000 009Сн |  |  | $\begin{gathered} \hline \text { BGR15 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { BGR05 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 00AOн | ISMK5 [R/W] B,----- ${ }^{\star 2}$ | $\begin{gathered} \text { ISBA5 [R/W] } \\ \underset{--H^{* 2}}{ } \end{gathered}$ | - |  |  |
| 0000 00A44 | $\begin{gathered} \text { SCR6 [R/W]/ } \\ \text { IBCR6 }[R, R / W] \\ \text { B,H,W*2 } \\ 0--00000 \end{gathered}$ | $\begin{gathered} \text { SMR6 [R/W] } \\ \text { B,H,W } \\ 000-0000 \end{gathered}$ | $\begin{gathered} \text { SSR6 [R,R/W] } \\ B, H, W \\ 0-000011 \end{gathered}$ | $\begin{gathered} \text { ESCR6 }[R / W] / \\ \text { IBSR6 } \\ {[R, R / W] B, H, W^{* 2}} \\ -0000000 \end{gathered}$ | Multi-function serial interface ch. 6 |
| 0000 00A8н | RDR6 [R] / TDR6 [W] B,H,---- 000000000 |  | $\begin{gathered} \hline \text { BGR16 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { BGR06 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 00ACH | ISMK6 [R/W] B, $\mathrm{H}^{\star 2}$ | $\begin{gathered} \text { ISBA6 [R/W] } \\ \mathrm{B}, \mathrm{H}^{\star 2} \\ ------ \end{gathered}$ | - |  |  |
| 0000 00B0н | $\begin{gathered} \text { SCR7 [R/W]/ } \\ \text { IBCR7 } \\ {[R, R / W] B, H, W^{* 2}} \\ 0--00000 \end{gathered}$ | $\begin{gathered} \text { SMR7 [R/W] } \\ \text { B,H,W } \\ 000-0000 \end{gathered}$ | $\begin{gathered} \text { SSR7 [R,R/W] } \\ \text { B,H,W } \\ 0-000011 \end{gathered}$ | $\begin{aligned} & \text { ESCR7 [R/W]/ } \\ & \text { IBSR7 [R,R/W] } \\ & \text { B,H,W*2 } \\ & -0000000 \end{aligned}$ | Multi-function serial interface ch. 7 |
| 0000 00B4н | RDR7 [R] / TDR7 [W] B,H,---- 000000000 |  | $\begin{gathered} \hline \text { BGR17 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { BGR07 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 00B8н | ISMK7 [R/W] B, $\mathrm{H}^{\star 2}$ | $\begin{gathered} \text { ISBA7 [R/W] } \\ \text { B,------- } \end{gathered}$ | - |  |  |
| 0000 00BCH | - |  |  |  | Reserved |

(Continued)

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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 00COH | $\begin{gathered} \hline \text { RDRM0 [R]/ } \\ \text { TDRM0 } \\ \text { [W] B,H,W } \\ 00000000 \end{gathered}$ | RDRM1 [R]/ <br> TDRM1 <br> [W] B,H,W <br> 00000000 | RDRM2 [R]/ TDRM2 <br> [W] B,H,W 00000000 | RDRM3 [R]/ TDRM3 <br> [W] B,H,W <br> 00000000 | Multi-function serial interface data register (mirror) |
| 0000 00C4н | RDRM4 [R]/ <br> TDRM4 <br> [W] B,H,W <br> 00000000 | RDRM5 [R] / <br> TDRM5 <br> [W] B,H,W <br> 00000000 | RDRM6 [R] / <br> TDRM6 <br> [W] B,H,W <br> 00000000 | RDRM7 [R] / <br> TDRM7 <br> [W] B,H,W <br> 00000000 |  |
| 0000 00C8H | SSEL0123 [R/----00 | - | $\underset{-----00}{\text { SSEL4567 [R/W] B }}$ | - | Multi-function serial interface serial clock selection |
| 0000 00CCH | - |  |  |  | Reserved |
| 0000 00DOн | $\begin{gathered} \text { SCR8 }[R / W] / \\ \text { IBCR8 } \\ {[R, \mathrm{R} / \mathrm{W}] \mathrm{B}, \mathrm{H}, \mathrm{~W}^{* 2}} \\ 0--00000 \end{gathered}$ | $\begin{gathered} \text { SMR8 [R/W] } \\ \text { B,H,W } \\ 000-0000 \end{gathered}$ | $\begin{gathered} \text { SSR8 [R,R/W] } \\ B, H, W \\ 0-000011 \end{gathered}$ | $\begin{gathered} \text { ESCR8 [R/W]/ } \\ \text { IBSR8 } \\ {[R, R / W] B, H, W^{\star 2}} \\ -0000000 \end{gathered}$ | Multi-function serial interface ch. 8 (FIFO) |
| 0000 00D4н | RDR8 [R] / TDR8 [W] B,H, W*1 |  | BGR18 [R/W] H,W 00000000 | $\begin{gathered} \text { BGR08 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 00D8н | ISMK8 [R/W] B, $\mathrm{H}^{* 2}$ $\qquad$ | $\text { ISBA8 [R/W] B, } \mathrm{H}^{* 2}$ | - |  |  |
| 0000 00DCH | $\begin{gathered} \text { FCR18 [R/W] } \\ \text { B,H,W } \\ ---00100 \end{gathered}$ | $\begin{gathered} \text { FCR08 [R,R/W] } \\ \text { B,H,W } \\ -0000000 \end{gathered}$ | $\begin{gathered} \text { FBYTE28 [R/W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { FBYTE18 [R/W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 00EOн | $\begin{gathered} \text { SCR9 }[\mathrm{R} / \mathrm{W}] / \\ \text { IBCR9 } \\ {[\mathrm{R}, \mathrm{R} / \mathrm{W}] \mathrm{B}, \mathrm{H}, \mathrm{~W}^{* 2}} \\ 0--00000 \end{gathered}$ | $\begin{gathered} \text { SMR9 [R/W] } \\ \text { B,H,W } \\ 000-0000 \end{gathered}$ | $\begin{gathered} \text { SSR9 [R,R/W] } \\ B, H, W \\ 0-000011 \end{gathered}$ | $\begin{gathered} \hline \text { ESCR9 [R/W]/ } \\ \text { IBSR9 }[R, R / W] \\ B, H, W^{*} 2 \\ -0000000 \end{gathered}$ | Multi-function serial interface ch. 9 (FIFO) |
| 0000 00E4н | RDR9 [R] / TDR9 [W] B,H,W*1 |  | $\begin{gathered} \text { BGR19 [R/W] H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { BGR09 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 00E8н | ISMK9 [R/W] B, $\mathrm{H}^{* 2}$ | ISBA9 [R/W] B, $\mathrm{H}^{* 2}$ | - |  |  |
| 0000 00ECH | $\begin{gathered} \text { FCR19 [R/W] } \\ \text { B,H,W } \\ ---00100 \end{gathered}$ | $\begin{gathered} \text { FCR09 [R,R/W] } \\ \text { B,H,W } \\ -0000000 \end{gathered}$ | $\begin{gathered} \text { FBYTE29 [R/W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { FBYTE19 [R/W] } \\ \text { B,H,W } \\ 000000000 \end{gathered}$ |  |

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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 00FOн | $\begin{gathered} \text { SCR10 }[\mathrm{R} / \mathrm{W}] / \\ \text { IBCR10 } \\ {[\mathrm{R}, \mathrm{R} / \mathrm{W}] \mathrm{B}, \mathrm{H}, \mathrm{~W} * 2} \\ 0--00000 \end{gathered}$ | $\begin{gathered} \text { SMR10 [R/W] } \\ \text { B,H,W } \\ 000-0000 \end{gathered}$ | $\begin{gathered} \text { SSR10 [R,R/W] } \\ B, H, W \\ 0-000011 \end{gathered}$ | $\begin{gathered} \hline \text { ESCR10 }[\mathrm{R} / \mathrm{W}] / \\ \text { IBSR10 } \\ {[\mathrm{R}, \mathrm{R} / \mathrm{W}] \mathrm{B}, \mathrm{H}, \mathrm{~W} * 2} \\ -0000000 \end{gathered}$ | Multi-function serial interface ch. 10 (FIFO) |
| 0000 00F4H | RDR10 [R] / TDR10 [W] B,H, W*1----00000000 |  | $\begin{gathered} \text { BGR110 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { BGR010 [R/W] } \\ \text { H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 00F8н | $\begin{gathered} \text { ISMK10 [R/W] } \\ \mathrm{B}, \mathrm{H}^{* 2} \\ ------ \end{gathered}$ | $\begin{gathered} \text { ISBA10 [R/W] } \\ \mathrm{B},-\mathrm{H}^{\star 2} \\ ------- \end{gathered}$ | - |  |  |
| 0000 00FCH | $\begin{gathered} \hline \text { FCR110 [R/W] } \\ \text { B,H,W } \\ ---00100 \end{gathered}$ | $\begin{gathered} \hline \text { FCR010 [R,R/W] } \\ \text { B,H,W } \\ -0000000 \end{gathered}$ | $\begin{gathered} \hline \text { FBYTE210[R/W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { FBYTE110 [R/W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 0100н | $\begin{gathered} \text { SCR11 [R/W] / } \\ \text { IBCR11 } \\ {[R, R / W] B, H, W^{* 2}} \\ 0--00000 \end{gathered}$ | $\begin{gathered} \text { SMR11 [R/W] } \\ \text { B,H,W } \\ 000-0000 \end{gathered}$ | $\begin{gathered} \text { SSR11 [R,R/W] } \\ \text { B,H,W } \\ 0-000011 \end{gathered}$ | $\begin{gathered} \text { ESCR11[R/W]/ } \\ \text { IBSR11 } \\ {[R, R / W] B, H, W^{* 2}} \\ -0000000 \end{gathered}$ | Multi-function serial interface ch. 11 (FIFO) |
| 0000 0104世 | RDR11[R] / TDR11[W] B,H, W*1 |  | $\begin{gathered} \text { BGR111 [R/W] } \\ H, W \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { BGR011 [R/W] } \\ H, W \\ 00000000 \end{gathered}$ |  |
| 0000 0108н | ISMK11 [R/W] $\mathrm{B}, \mathrm{H}^{* 2}$ -------- | $\begin{gathered} \hline \text { ISBA11 [R/W] } \\ \mathrm{B},-\mathrm{H}^{* 2} \\ ------ \end{gathered}$ | - |  |  |
| 0000 010Сн | $\begin{gathered} \text { FCR111 [R/W] } \\ \text { B,H,W } \\ ---00100 \end{gathered}$ | $\begin{gathered} \hline \text { FCR011 [R,R/W] } \\ \text { B,H,W } \\ -0000000 \end{gathered}$ | $\begin{gathered} \hline \text { FBYTE211 [R/W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { FBYTE111[R/W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ |  |
| 0000 0110н | $\begin{gathered} \hline \text { EIRR1 [R/W] } \\ B, H, W \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { ENIR1 [R/W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ | ELVR1 [R/W] B,H,W 0000000000000000 |  | External interrupt 8 to 15 |
| 0000 0114H | $\begin{gathered} \hline \text { EIRR2 }[\mathrm{R} / \mathrm{W}] \\ \mathrm{B}, \mathrm{H}, \mathrm{~W} \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { ENIR2 }[\mathrm{R} / \mathrm{W}] \\ \mathrm{B}, \mathrm{H}, \mathrm{~W} \\ 00000000 \end{gathered}$ | ELVR2 [R/W] B,H,W 0000000000000000 |  | External interrupt 16 to 23 |
| 0000 0118н | $\begin{gathered} \text { EIRR3 [R/W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { ENIR3 [R/W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ | ELVR3 [R/W] B,H,W 0000000000000000 |  | External interrupt 24 to 31 |
| 0000 011CH | - |  |  |  | Reserved |

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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 0120н | ADCRO $[R / W] B, H$ $000-0000$ | $\begin{gathered} \hline \text { ADSRO }[R, R / W] \\ B, H \\ 00---000 \end{gathered}$ | - |  | A/D converter unit 0 |
| 0000 0124H | $\begin{gathered} \text { SCCRO }[R, R / W] B, H \\ 1000-000 \end{gathered}$ | $\begin{gathered} \hline \text { SFNSO [R/W] B,H } \\ ---0000 \end{gathered}$ | $\begin{gathered} \text { SCFDO }[R] B, H \\ X X X X X X X X X-X X X X \end{gathered}$ |  |  |
| 0000 0128 | - |  | $\begin{gathered} \text { SCIS10 [R/W] } \\ \text { B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { SCIS00 [R/W] B,H } \\ 00000000 \end{gathered}$ |  |
| 0000 012Cн | $\begin{gathered} \text { PCCRO }[R, R / W] B, H \\ 1000-000 \end{gathered}$ | $\begin{gathered} \text { PFNSO[R/W] B,H } \\ ----00 \end{gathered}$ | $\begin{gathered} \text { PCFDO[R]B,H } \\ X X X X X X X X X X X X X \end{gathered}$ |  |  |
| 0000 0130н | PCISO [R/W] B 00000000 | - | $\begin{gathered} \text { CMPDO [R/W] } \\ \text { B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { CMPCRO [R/W] } \\ \text { B,H } \\ 00000000 \end{gathered}$ |  |
| 0000 0134 | - |  | $\begin{gathered} \hline \text { ADSS10 }[\mathrm{R} / \mathrm{W}] \\ \text { B, H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { ADSS00 }[R / W] B, H \\ 00000000 \end{gathered}$ |  |
| 0000 0138 | $\begin{gathered} \text { ADST00 [R/W] B,H } \\ 00100000 \end{gathered}$ | $\begin{array}{\|c} \hline \text { ADST10 [R/W] B,H } \\ 00100000 \end{array}$ | $\begin{gathered} \text { ADCTO [R/W] B } \\ ---111 \end{gathered}$ | - |  |
| 0000 013CH | - |  |  |  | Reserved |
| 0000 0140н | $\begin{gathered} \text { BTOTMR [R] H } \\ 0000000000000000 \end{gathered}$ |  | BTOTMCR [R/W] B,H -0000000 00000000 |  | Base timer ch. 0 |
| 0000 0144H | - | $\begin{gathered} \text { BTOSTC [R/W] B } \\ 0000-000 \end{gathered}$ |  | - |  |
| 0000 0148н | BTOPCSR / BTOPRLL [R/W] H XXXXXXXX XXXXXXXX |  | BTOPDUT / BTOPRLH / BTODTBF [R/W] H XXXXXXXX XXXXXXXX |  |  |
| 0000 014CH | - |  |  |  |  |
| 0000 0150н | BT1TMR [R] H0000000000000000 |  | $\begin{aligned} & \hline \text { BT1TMC } \\ & -000000 \end{aligned}$ | $\begin{aligned} & \hline \mathrm{R}[\mathrm{R} / \mathrm{W}] \mathrm{B}, \mathrm{H} \\ & 000000000 \end{aligned}$ | Base timer ch. 1 |
| 0000 0154H | - | $\begin{gathered} \text { BT1STC [R/W] B } \\ 0000-000 \end{gathered}$ |  | - |  |
| 0000 0158н | BT1PCSR / BT1PRLL [R/W] H XXXXXXXX XXXXXXXX |  | BT1PDUT / BT1PRLH / BT1DTBF [R/W] H XXXXXXXX XXXXXXXX |  |  |
| 0000 015CH | - |  |  |  |  |

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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 0160н | BT2TMR [R] H 0000000000000000 |  | BT2TMCR [R/W] B,H -000000000000000 |  | Base timer ch. 2 |
| 0000 0164н | - | $\begin{gathered} \hline \text { BT2STC }[R / W] \text { B } \\ 0000-000 \end{gathered}$ |  |  |  |
| 0000 0168н | BT2PCSR / BT2PRLL [R/W] H XXXXXXXX XXXXXXXX |  | BT2PDUT / BT2PRLH / BT2DTBF [R/W] H XXXXXXXX XXXXXXXX |  |  |
| 0000 016CH | - |  |  |  |  |
| 0000 0170н | $\begin{gathered} \text { BT3TMR [R] H } \\ 0000000000000000 \end{gathered}$ |  | BT3TMCR [R/W] B,H-000000000000000 |  | Base timer ch. 3 |
| 0000 0174н | - | BT3STC [R/W] B $0000-000$ |  |  |  |
| 0000 0178н | BT3PCSR / BT3PRLL [R/W] H XXXXXXXX XXXXXXXX |  | BT3PDUT / BT3PRLH / BT3DTBF [R/W] H <br> XXXXXXXX XXXXXXXX |  |  |
| 0000 017С ${ }_{\text {H }}$ | BTSEL0123 [R/W] B 00000000 | - |  |  |  |
| 0000 0180н | $\begin{gathered} \hline \text { DACRO }[\mathrm{R} / \mathrm{W}] \\ \mathrm{B}, \mathrm{H}, \mathrm{~W} \\ -----0 \end{gathered}$ | $\begin{gathered} \hline \text { DADRO [R/W] } \\ \text { B,H,W } \\ \text { XXXXXXXX } \end{gathered}$ | $\begin{gathered} \hline \text { DACR1 [R/W] } \\ \text { B,H,W } \\ -----0 \end{gathered}$ | $\begin{gathered} \hline \text { DADR1 [R/W] } \\ \text { B,H,W } \\ \text { XXXXXXXX } \end{gathered}$ | D/A converter |
| $\begin{gathered} 00000184_{H} \\ \text { to } \\ 000018 C_{H} \end{gathered}$ | - |  |  |  |  |
| $\begin{aligned} & 0000 \text { 0190н } \\ & \text { to } \\ & 0000 \text { 01А8 } \end{aligned}$ | - |  |  |  | Reserved |
| 0000 01ACH | ADCHE [R/W] B,H,W-11111111111111111111111111111 |  |  |  | A/D channel enable |
| 0000 01B0н | $\begin{gathered} \text { IRPROH }[R] B \\ 000----- \end{gathered}$ | - | $\begin{aligned} & \text { IRPR1H [R] B,H } \\ & 000-000- \end{aligned}$ | $\begin{gathered} \text { IRPR1L [R] B,H } \\ 000-000- \end{gathered}$ | Interrupt request batch read function |
| 0000 01B4н | $\begin{gathered} \text { IRPR2H }[R] B, H, W \\ 0000---- \end{gathered}$ | $\begin{array}{\|c\|} \hline \text { IRPR2L }[R] B, H, W \\ 000----- \end{array}$ | $\left\lvert\, \begin{gathered} \text { IRPR3H }[R] \text { B,H,W } \\ 0000---- \end{gathered}\right.$ | $\begin{aligned} & \hline \text { IRPR3L }[R] \text { B,H,W } \\ & 00000--- \end{aligned}$ |  |
| 0000 01B8н | $\begin{gathered} \text { IRPR4H }[R] B, H, W \\ 0000---- \end{gathered}$ | $\begin{aligned} & \text { IRPR4L [R] B,H,W } \\ & 000000-\mathrm{H} \end{aligned}$ | $\begin{array}{\|c\|} \hline \text { IRPR5H [R] B,H,W } \\ 0000---- \end{array}$ | $\begin{aligned} & \text { IRPR5L [R] B,H,W } \\ & 0000---- \end{aligned}$ |  |
| 0000 01BCH | $\begin{aligned} & \text { IRPR6H [R] B,H,W } \\ & 0000--- \end{aligned}$ | $\begin{gathered} \text { IRPR6L [R] B,H,W } \\ 0000---\mathrm{W} \end{gathered}$ | $\begin{array}{\|c} \text { IRPR7H }[R] B, H, W \\ 0000---- \end{array}$ | $\begin{aligned} & \text { IRPR7L [R] B,H,W } \\ & 0000 \text {---- } \end{aligned}$ |  |

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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 01C0н | RCRHO [W] H,W 00000000 | $\begin{gathered} \hline \text { RCRLO [W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ | UDCRHO [R] H,W 00000000 | $\begin{gathered} \hline \text { UDCRLO }[R] \\ \text { B,H,W } \\ 00000000 \end{gathered}$ | Up/down counter ch. 0 |
| 0000 01C4H | CCRO [R,R/W] B,H 00000000-0001000 |  | - | $\begin{gathered} \text { CSR0 }[R, R / W] B \\ 00000000 \end{gathered}$ |  |
| 0000 01С8 | - |  |  |  |  |
| 0000 01СС | - |  |  |  | Reserved |
| 0000 01D0н | RCRH1 [W] H,W 00000000 | $\begin{aligned} & \text { RCRL1 [W] } \\ & \text { B,H,W } \\ & 00000000 \end{aligned}$ | UDCRH1 [R] H,W 00000000 | $\begin{aligned} & \text { UDCRL1 [R] } \\ & \text { B,H,W } \\ & 00000000 \end{aligned}$ | Up/down counter ch. 1 |
| 0000 01D4н | CCR1 [R,R/W] B,H 00000000-0001000 |  | - | $\begin{gathered} \hline \text { CSR1 }[R, R / W] B \\ 00000000 \end{gathered}$ |  |
| 0000 01D8 | - |  |  |  |  |
| 0000 01DCH | - |  |  |  | Reserved |
| 0000 01E0н | $\begin{aligned} & \text { RCRH2 [W] H,W } \\ & 00000000 \end{aligned}$ | $\begin{gathered} \hline \text { RCRL2 [W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ | UDCRH2 [R]H,W 00000000 | $\begin{aligned} & \text { UDCRL2 [R] } \\ & \text { B,H,W } \\ & 00000000 \\ & \hline \end{aligned}$ | Up/down counterch. 2 |
| 0000 01E4н | CCR2 [R,R/W] B,H 00000000-0001000 |  | - | $\begin{gathered} \hline \text { CSR2 }[R, R / W] B \\ 00000000 \end{gathered}$ |  |
| 0000 01E8H | - |  |  |  |  |
| 0000 01ECH | - |  |  |  | Reserved |
| 0000 01FOH | $\begin{gathered} \text { RCRH3 [W] H,W } \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { RCRL3 [W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ | UDCRH3 [R] H,W 00000000 | $\begin{gathered} \hline \text { UDCRL3 [R] } \\ \text { B,H,W } \\ 000000000 \end{gathered}$ | Up/down counterch. 3 |
| 0000 01F4н | CCR3 [R,R/W] B,H 00000000-0001000 |  | - | $\begin{gathered} \text { CSR3 }[R, R / W] B \\ 00000000 \end{gathered}$ |  |
| 0000 01F8н | - |  |  |  |  |
| 0000 01FCH | - |  |  |  | Reserved |
| 0000 0200н | CPCLRO [R/W] W111111111111111111111111111111 |  |  |  | 32-bit <br> Free-run timer ch. 0 |
| 0000 0204н | TCDTO [R/W] W00000000000000000000000000000000 |  |  |  |  |
| 0000 0208н | $\underset{0----00}{\text { TCCSHO }}$ | $\begin{gathered} \hline \text { TCCSLO [R/W] } \\ \text { B,H } \\ -1-00000 \end{gathered}$ |  |  |  |

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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 020CH | IPCP0 [R] WXXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |  |  |  |  |
| 0000 0210н | IPCP1 [R] W <br> XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |  |  |  |  |
| 0000 0214н | IPCP2 [R] W <br> XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |  |  |  | 32-bit Input capture ch. 0 to ch. 3 |
| 0000 0218н | IPCP3 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |  |  |  |  |
| 0000 021CH | - | $\begin{gathered} \hline \text { ICS01 [R/W] B } \\ 00000000 \end{gathered}$ | - | $\begin{gathered} \hline \text { ICS23 [R/W] B } \\ 00000000 \end{gathered}$ |  |
| 0000 0220н | IPCP4 [R] W <br> XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |  |  |  |  |
| 0000 0224н | IPCP5 [R] W <br> XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |  |  |  |  |
| 0000 0228н | IPCP6 [R] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |  |  |  | 32-bit Input capture ch. 4 to ch. 7 |
| 0000 022C | IPCP7 [R] W <br> XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |  |  |  |  |
| 0000 0230н | - | $\begin{gathered} \hline \text { ICS45 [R/W] B } \\ 00000000 \end{gathered}$ | - | $\begin{aligned} & \hline \text { ICS67 [R/W] B } \\ & 00000000 \end{aligned}$ |  |
| 0000 0234н | OCCPO [R/W] W00000000000000000000000000000000 |  |  |  |  |
| 0000 0238 | OCCP1 [R/W] W00000000000000000000000000000000 |  |  |  |  |
| 0000 023C | OCCP2 [R/W] W00000000000000000000000000000000 |  |  |  | 32-bit Output compare |
| 0000 0240н | OCCP3 [R/W] W00000000000000000000000000000000 |  |  |  | ch. 0 to ch. 3 |
| 0000 0244н | $\begin{gathered} \text { OCSH1 [R/W] } \\ \mathrm{B}, \mathrm{H}, \mathrm{~W} \\ -----00 \end{gathered}$ | $\begin{gathered} \text { OCSLO [R/W] } \\ \text { B,H,W } \\ 0000--00 \end{gathered}$ | $\begin{gathered} \text { OCSH3 [R/W] } \\ \text { B,H,W } \\ ---0--00 \end{gathered}$ | $\begin{gathered} \text { OCSL2 [R/W] } \\ \text { B,H,W } \\ 0000--00 \end{gathered}$ |  |

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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 0248H | OCCP4 [R/W] W0000000000000000000000000000000 |  |  |  | 32-bit <br> Output compare ch. 4 to ch. 7 |
| 0000 024CH | OCCP5 [R/W] W00000000000000000000000000000000 |  |  |  |  |
| 0000 0250н | OCCP6 [R/W] W00000000000000000000000000000000 |  |  |  |  |
| 0000 0254н | OCCP7 [R/W] W00000000000000000000000000000000 |  |  |  |  |
| 0000 0258н | $\begin{gathered} \hline \text { OCSH5 [R/W] } \\ \text { B,H,W } \\ -----00 \end{gathered}$ | $\begin{gathered} \text { OCSL4 [R/W] } \\ \text { B,H,W } \\ 0000--00 \end{gathered}$ | $\begin{gathered} \text { OCSH7 [R/W] } \\ \text { B,H,W } \\ ---0-00 \end{gathered}$ | $\begin{gathered} \hline \text { OCSL6 [R/W] } \\ \text { B,H,W } \\ 0000--00 \end{gathered}$ |  |
| 0000 025CH | FRTSEL $\underset{----00}{ }$ |  | - |  | Free-run timer selector |
| 0000 0260н | CPCLR1 [R/W] W111111111111111111111111111111 |  |  |  | 32-bit <br> Free-run timer ch. 1 |
| 0000 0264н | TCDT1 [R/W] W00000000000000000000000000000000 |  |  |  |  |
| 0000 0268н | $\begin{gathered} \text { TCCSH1 [R/W] B,H } \\ 0---00 \end{gathered}$ | $\begin{gathered} \text { TCCSL1 [R/W] } \\ \text { B,H } \\ -1-00000 \end{gathered}$ | - |  |  |
| $\begin{gathered} 0000 \text { 026CH } \\ \text { to } \\ 0000 \stackrel{031 C_{H}}{ } \end{gathered}$ | - |  |  |  | Reserved |
| 0000 0320н | $\begin{aligned} & \text { FCTLR [R/W] H } \\ & -0-1011 \text {------- } \end{aligned}$ |  | - | $\underset{\substack{\text { FSTR }----1}}{ }$ | Flash memory control |
| $\begin{gathered} 0000 \text { 0324н } \\ \text { to } \\ 0000 \text { 0334н } \end{gathered}$ | - |  |  |  | Reserved |
| 0000 0338н | - |  | WREN [R/W] B,H 0000000000000000 |  | Wild register |
| 0000 033CH | - |  |  |  |  |
| $\begin{gathered} 0000 \text { 0340н } \\ \text { to } \\ 0000 \stackrel{037 \mathrm{C}_{\mathrm{H}}}{ } \end{gathered}$ | - |  |  |  | Reserved |

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## MB91625 Series


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## MB91625 Series


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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 0400н | DDR0 [R/W] B,H 00000000 | $\begin{gathered} \hline \text { DDR1 [R/W] B,H } \\ 00000000 \end{gathered}$ | DDR2 [R/W] B,H 00000000 | $\begin{gathered} \hline \text { DDR3 }[\mathrm{R} / \mathrm{W}] \mathrm{B}, \mathrm{H} \\ 00000000 \end{gathered}$ | Data direction register |
| 0000 0404н | $\begin{gathered} \text { DDR4 [R/W] B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { DDR5 [R/W] B,H } \\ 00000000 \end{gathered}$ | DDR6 [R/W] B,H 00000000 | $\begin{gathered} \hline \text { DDR7[R/W] B,H } \\ 00000000 \end{gathered}$ |  |
| 0000 0408н | DDR8 [R/W] B,H 00000000 | $\underset{----000}{ }$ | DDRA [R/W] B 00000000 | - |  |
| $\begin{aligned} & 0000 \text { to } 040 \mathrm{C}_{\mathrm{H}} \\ & 0000 \text { 0410н } \end{aligned}$ | - |  |  |  |  |
| 0000 0414H | $\begin{gathered} \text { DDRK [----000 } \\ \hline \end{gathered}$ | - |  |  |  |
| $\begin{gathered} 0000 \text { 0418н } \\ \text { to } \\ 0000{ }^{041 C_{H}} \end{gathered}$ | - |  |  |  |  |
| 0000 0420н | PCR0 [R/W] B,H 00000000 | $\begin{gathered} \hline \text { PCR1 [R/W] B,H } \\ 00000000 \end{gathered}$ | - |  | Pull-up control register |
| 0000 0424н | - | PCR5 [R/W] B 00000000 | $\begin{gathered} \text { PCR6 [R/W] B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { PCR7[R/W] B,H } \\ 00000000 \end{gathered}$ |  |
| 0000 0428н | PCR8 [R/W] B,H 00000000 | $\underset{----000}{ }$ | PCRA [R/W] B 00000000 | - |  |
| $\begin{gathered} 0000 \text { 042CH } \\ \text { to } \\ 0000430 \text { н } \end{gathered}$ | - |  |  |  |  |
| 0000 0434н | PCRK [R/W] B -----0-- | - |  |  |  |
| $\begin{gathered} 0000 \text { to } \\ \text { to } \\ 0000{ }^{043 C_{H}} \end{gathered}$ | - |  |  |  |  |

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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 0440н | $\begin{gathered} \hline \text { ICR00 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR01 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR02 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR03 }[\mathrm{R}, \mathrm{R} / \mathrm{W}] \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | Interrupt control |
| 0000 04444 | $\begin{gathered} \hline \text { ICR04 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR05 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR06 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR07 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ |  |
| 0000 0448н | $\begin{gathered} \hline \text { ICR08 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR09 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR10 }[R, R / W] \\ B, H, W \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR11 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ |  |
| 0000 044CH | $\begin{gathered} \text { ICR12 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \text { ICR13 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \text { ICR14 }[R, R / W] \\ B, H, W \\ ---11111 \end{gathered}$ | $\begin{gathered} \text { ICR15 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ |  |
| 0000 0450н | $\begin{gathered} \hline \text { ICR16 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR17 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR18 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR19 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ |  |
| 0000 0454н | $\begin{gathered} \hline \text { ICR20 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR21 [R,R/W] } \\ \text { B,H,W } \\ --11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR22 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR23 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ |  |
| 0000 0458н | $\begin{gathered} \text { ICR24 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \text { ICR25 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \text { ICR26 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \text { ICR27 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ |  |
| 0000 045CH | $\begin{gathered} \hline \text { ICR28 }[\mathrm{R}, \mathrm{R} / \mathrm{W}] \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR29 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR30 }[\mathrm{R}, \mathrm{R} / \mathrm{W}] \\ \mathrm{B}, \mathrm{H}, \mathrm{~W} \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR31 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ |  |
| 0000 0460н | $\begin{gathered} \hline \text { ICR32 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR33 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR34 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR35 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ |  |
| 0000 0464н | $\begin{gathered} \hline \text { ICR36 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR37 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR38 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR39 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ |  |
| 0000 0468н | $\begin{gathered} \hline \text { ICR40 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR41 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR42 }[\mathrm{R}, \mathrm{R} / \mathrm{W}] \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR43 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ |  |
| 0000 046CH | $\begin{gathered} \hline \text { ICR44 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR45 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR46 [R,R/W] } \\ \text { B,H,W } \\ ---11111 \end{gathered}$ | $\begin{gathered} \hline \text { ICR47 [R,R/W] } \\ \text { B,H,W } \\ --11111 \end{gathered}$ |  |
| $\begin{aligned} & 0000 \text { 0470н } \\ & \text { to } \\ & 0000047 \text { C }_{H} \end{aligned}$ | - |  |  |  | Reserved |

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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 0480н | $\underset{11-X---X^{\star 3}}{\operatorname{RSTRR}}[\mathrm{R}] \mathrm{B}, \mathrm{H}, \mathrm{~W}$ | $\begin{gathered} \hline \text { RSTCR [R/W] } \\ \text { B,H,W } \\ 000----0 \end{gathered}$ | $\begin{gathered} \hline \text { STBCR [R/W] } \\ B, H, W \\ 0000--11 \end{gathered}$ | $\begin{gathered} \hline \text { SLPRR [R/W] } \\ \text { B,H,W } \\ 00000000 \end{gathered}$ | Reset control/ Power consumption control |
| 0000 0484н | - |  |  |  |  |
| 0000 0488н | DIVRO [R/W] B,H $000----$ | - | DIVR2 [R/W] B $0011----$ | - | Clock division control |
| 0000 048CH | - |  |  |  |  |
| 0000 0490н | $\begin{gathered} \hline \text { IORR0 [R/W] } \\ B, H, W \\ -0000000 \end{gathered}$ | $\begin{gathered} \hline \text { IORR1 [R/W] } \\ B, H, W \\ -0000000 \end{gathered}$ | $\begin{gathered} \text { IORR2 [R/W] } \\ \text { B,H,W } \\ -0000000 \end{gathered}$ | $\begin{gathered} \text { IORR3 [R/W] } \\ \text { B,H,W } \\ -0000000 \end{gathered}$ | Peripheral DMA transmission re quest control |
| 0000 04944 | $\begin{gathered} \text { IORR4 }[R / W] \\ B, H, W \\ -0000000 \end{gathered}$ | $\begin{gathered} \text { IORR5 [R/W] } \\ B, H, W \\ -0000000 \end{gathered}$ | $\begin{gathered} \text { IORR6 [R/W] } \\ B, H, W \\ -0000000 \end{gathered}$ | $\begin{gathered} \text { IORR7 [R/W] } \\ B, H, W \\ -0000000 \end{gathered}$ |  |
| $\begin{array}{\|c} \hline 0000 \text { 0498н } \\ \text { to } \\ 0000 \text { 049CH }^{2} \end{array}$ | - |  |  |  | Reserved |
| 0000 04AOH | $\begin{gathered} \text { PFR0 [R/W] B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { PFR1 [R/W] B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { PFR2 [R/W] B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { PFR3 [R/W] B,H } \\ 00000000 \end{gathered}$ | Port function register |
| 0000 04A4н | $\begin{gathered} \hline \text { PFR4 [R/W] B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { PFR5 [R/W] B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \hline \text { PFR6 [R/W] B,H } \\ 00-00-0- \end{gathered}$ | $\begin{gathered} \hline \text { PFR7[R/W] B,H } \\ 00000000 \end{gathered}$ |  |
| 0000 04A8н | PFR8 [R/W] B 00000000 | - | PFRA [R/W] B $00-00000$ | - |  |
| $\begin{array}{\|c} \hline 00004 \mathrm{ACH} \\ \text { to } \\ 0000 \text { 04B4H } \end{array}$ | - |  |  |  |  |

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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 04B8н | $\begin{gathered} \hline \text { EPFRO [R/W] B,H } \\ --000000 \end{gathered}$ | $\underset{\substack{\text { EPFR1 [R/W] B,H } \\-000000}}{ }$ | $\begin{gathered} \text { EPFR2 [R/W] B,H } \\ --000000 \end{gathered}$ | EPFR3 $[\mathrm{R} / \mathrm{W}] \mathrm{B}, \mathrm{H}$ --000000 | Extended port function register |
| 0000 04BCH | $\begin{gathered} \text { EPFR4 }[R / W] B, H \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { EPFR5 }[R / W] B, H \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { EPFR6 [R/W] B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { EPFR7 [R/W] B,H } \\ ---00000 \end{gathered}$ |  |
| 0000 04C0н | $\begin{gathered} \hline \text { EPFR8 [R/W] B,H } \\ --00000 \end{gathered}$ | $\underset{---00000}{\text { EPFR9 }[R / W]} \mathrm{B}, \mathrm{H}$ | EPFR10 [R/W] B,H ---00000 | EPFR11 [R/W] B,H ---00000 |  |
| 0000 04C4н | $\begin{gathered} \text { EPFR12 [R/W] B,H } \\ ---00000 \end{gathered}$ | $\begin{gathered} \text { EPFR13 }[\mathrm{R} / \mathrm{W}] \mathrm{B}, \mathrm{H} \\ ---00000 \end{gathered}$ | $\begin{gathered} \text { EPFR14 [R/W] B,H } \\ ---00000 \end{gathered}$ | $\underset{---00000}{ }$ |  |
| 0000 04C8н | $\begin{gathered} \text { EPFR16 [R/W] B,H } \\ ---00000 \end{gathered}$ | $\begin{gathered} \text { EPFR17 [R/W] B,H } \\ ---00000 \end{gathered}$ | EPFR18 [R/W] B,H 00000000 | EPFR19 [R/W] B,H -0000001 |  |
| 0000 04ССн | $\begin{gathered} \text { EPFR20 }[\mathrm{R} / \mathrm{W}] \mathrm{B}, \mathrm{H} \\ --000000 \end{gathered}$ | $\begin{gathered} \text { EPFR21 [R/W] B,H } \\ --000000 \end{gathered}$ | $\begin{gathered} \text { EPFR22 [R/W] B,H } \\ --000000 \end{gathered}$ | $\underset{--000000}{\text { EPFR23 [R/W] B,H }}$ |  |
| 0000 04D0н | $\underset{--00000}{\text { EPFR24 [R/W] B,H }}$ | $\begin{gathered} \text { EPFR25 }[R / W] B, H \\ --000000 \end{gathered}$ | $\begin{gathered} \text { EPFR26 [R/W] B,H } \\ --000000 \end{gathered}$ | $\underset{--000000}{ } \mathrm{EPFR} 2 \mathrm{R} / \mathrm{W}] \mathrm{B}, \mathrm{H}$ |  |
| 0000 04D4н | $\begin{gathered} \text { EPFR28 [R/W] B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { EPFR29 [R/W] B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { EPFR30 [R/W] B,H } \\ ----0000 \end{gathered}$ | $\begin{gathered} \text { EPFR31 [R/W] B,H } \\ -0000000 \end{gathered}$ |  |
| 0000 04D8н | $\begin{gathered} \text { EPFR32 [R/W] B,H } \\ 00000000 \end{gathered}$ | $\begin{gathered} \text { EPFR33 [R/W] B,H } \\ --000000 \end{gathered}$ | $\begin{gathered} \hline \text { EPFR34 }[\mathrm{R} / \mathrm{W}] \mathrm{B} \\ -0000000 \end{gathered}$ | - |  |
| 0000 04DCH | - - |  |  |  |  |
| $\begin{gathered} 0000 \text { 04ЕОн } \\ \text { to } \\ 0000 \begin{array}{c} 04 E C H \end{array} \end{gathered}$ | - |  |  |  | Reserved |
| 0000 04FOH | $\begin{gathered} \hline \text { ICSELO [R/W] } \\ \text { B,H,W } \\ ----000 \end{gathered}$ | $\begin{gathered} \text { ICSEL1 [R/W] } \\ \text { B,H,W } \\ ----000 \end{gathered}$ | $\begin{gathered} \text { ICSEL2 [R/W] } \\ \mathrm{B}, \mathrm{H}, \mathrm{~W} \\ ----000 \end{gathered}$ | $\begin{gathered} \text { ICSEL3 [R/W] } \\ \text { B,-H,W } \\ ----000 \end{gathered}$ | DMA start request clear select function |
| 0000 04F4H | $\begin{gathered} \text { ICSEL4 [R/W] } \\ \text { B,H,W } \\ -----00 \end{gathered}$ | $\begin{gathered} \text { ICSEL5 [R/W] } \\ \text { B,H,W } \\ ----000 \end{gathered}$ | $\begin{gathered} \text { ICSEL6 [R/W] } \\ \text { B,-H,W } \\ ----00 \end{gathered}$ | $\begin{gathered} \text { ICSEL7 [R/W] } \\ B,------0 \\ ---0 \end{gathered}$ |  |
| 0000 04F8H | $\begin{gathered} \text { ICSEL8 [R/W] } \\ \text { B,-H,W } \\ ----00 \end{gathered}$ | $\begin{gathered} \hline \text { ICSEL9 [R/W] } \\ \text { B,H,W } \\ ----000 \end{gathered}$ | $\begin{gathered} \hline \text { ICSEL10 [R/W] } \\ \text { B,H,W } \\ ----0000 \end{gathered}$ | $\begin{gathered} \hline \text { ICSEL11 [R/W] } \\ \text { B,H,W } \\ ----0000 \end{gathered}$ |  |
| 0000 04FCH | $\begin{gathered} \hline \text { ICSEL12 [R/W] } \\ \text { B,H } \\ ---0000 \end{gathered}$ | $\begin{gathered} \text { ICSEL13 [R/W] } \\ \text { B,-H } \\ ----0-0 \end{gathered}$ | $\begin{gathered} \hline \text { ICSEL14 [R/W] } \\ \text { B } \\ ----00 \end{gathered}$ | - |  |

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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| $\begin{aligned} & 0000 \text { 0500н } \\ & \text { to } \\ & 0000 \stackrel{050 \mathrm{C}_{\mathrm{H}}}{ } \end{aligned}$ | - |  |  |  | Reserved |
| 0000 0510н | $\begin{gathered} \hline \text { CSELR [R/W] } \\ \text { B,H,W } \\ 001---00 \end{gathered}$ | $\begin{gathered} \hline \text { CMONR [R] } \\ \text { B,H,W } \\ 001---00 \end{gathered}$ | $\begin{gathered} \hline \text { MTMCR [R/W] } \\ \text { B,H,W } \\ 00001111 \end{gathered}$ | $\begin{gathered} \hline \text { STMCR [R/W] } \\ B, H, W \\ 0000-111 \end{gathered}$ | Clock generation/ |
| 0000 0514н | $\begin{aligned} & \hline \text { PLLCR [R/W] B,H } \\ & --00000011110000 \end{aligned}$ |  | $\begin{gathered} \text { CSTBR [R/W] B } \\ -0000000 \end{gathered}$ | - | Sub timer |
| 0000 0518н | $\begin{aligned} & \hline \text { WCRD [R] B,H } \\ & --000000 \end{aligned}$ | $\begin{gathered} \text { WCRL [R/W] B,H } \\ --000000 \end{gathered}$ | $\begin{gathered} \text { WCCR [R,R/W] B } \\ 00--0000 \end{gathered}$ | - | Clock counter |
| $\begin{gathered} 00000^{051 C_{H}} \\ \text { to } \\ 0000 \text { 0BFCH } \end{gathered}$ | - |  |  |  | Reserved |
| 0000 0СС0~ | $\begin{gathered} \text { DCCR0 [R/W] W } \\ 0----000--0000000000-000000 \end{gathered}$ |  |  |  | DMAC |
| 0000 0C04H |  |  | DTCRO [R/W] H0000000000000000 |  |  |
| 0000 0С08н | DSARO [R/W] WXXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |  |  |  |  |
| 0000 0С0Сн | DDAR0 [R/W] WXXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |  |  |  |  |
| 0000 0C10н | $\begin{gathered} \hline \text { DCCR1 [R/W] W } \\ 0----000--0000000000-000000 \end{gathered}$ |  |  |  |  |
| 0000 OC14 | $\begin{gathered} \hline \text { DCSR1 } \\ 0------1 \end{gathered}$ | 2,R/W] H | $\begin{array}{r} \hline \text { DTCR1 } \\ 00000000 \end{array}$ | R/W] H 0000000 |  |
| 0000 OC18 ${ }^{\text {H }}$ | XXX | $\begin{array}{r} \text { DSAR1 } \\ \mathrm{XXXX} \mathrm{XXXXXXX} \end{array}$ | R/W] W $X X X X X X X X ~ X X X X X$ |  |  |
| 0000 0С1С |  | $\begin{array}{r} \text { DDAR1 } \\ \mathrm{XXXX} \mathrm{XXXXXXXX} \end{array}$ | $\begin{aligned} & \text { R/W] W } \\ & \text { XXXXXXXX XXXX } \end{aligned}$ |  |  |
| 0000 0С20н |  | $\begin{array}{r} \text { DCCR2 } \\ 0----000--0000 \end{array}$ | $\begin{aligned} & \text { R/W] W } \\ & 10000000-000000 \end{aligned}$ |  |  |
| 0000 OC24H | $\begin{array}{r} \text { DCSR2 } \\ 0------1 \end{array}$ | Q,R/W] H | $\begin{gathered} \text { DTCR2 } \\ 00000000 \end{gathered}$ | $\begin{aligned} & \text { Z/W] H } \\ & 10000000 \end{aligned}$ |  |
| 0000 0C28 ${ }^{\text {H }}$ | DSAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |  |  |  |  |
| 0000 0С2Сн | DDAR2 [R/W] W XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX |  |  |  |  |
| 0000 0С30н | $\begin{gathered} \hline \text { DCCR3 [R/W] W } \\ 0----000--0000000000-000000 \end{gathered}$ |  |  |  |  |
| 0000 0C34 | $\begin{gathered} \text { DCSR3 [R,R/W] H } \\ 0---------000 \end{gathered}$ |  | DTCR3 [R/W] H0000000000000000 |  |  |

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## MB91625 Series


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## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 0DF8н |  |  |  |  | DMAC |
| $\begin{gathered} 0000 \text { ODFCH } \\ \text { to } \\ 0000 \begin{array}{c} 0 \mathrm{~F} 3 \mathrm{C}_{\mathrm{H}} \end{array} \end{gathered}$ | - |  |  |  | Reserved |
| 0000 0F40н | $\begin{gathered} \text { BT4TMR [R] H } \\ 0000000000000000 \end{gathered}$ |  | BT4TMCR [R/W] B,H -0000000 00000000 |  | Base timer ch. 4 |
| 0000 0F44н | - | $\begin{gathered} \text { BT4STC [R/W] B } \\ 0000-000 \end{gathered}$ |  |  |  |
| 0000 0F48н | BT4PCSR / BT4PRLL [R/W] H XXXXXXXX XXXXXXXX |  | BT4PDUT / BT4PRLH / BT4DTBF [R/W] H XXXXXXXX XXXXXXXX |  |  |
| 0000 0F4CH | - |  |  |  |  |
| 0000 0F50н | $\begin{gathered} \text { BT5TMR [R] H } \\ 0000000000000000 \end{gathered}$ |  |  |  | Base timer ch. 5 |
| 0000 0F54н | - | BT5STC [R/W] B $0000-000$ |  |  |  |
| 0000 0F58н | BT5PCSR / BT5PRLL [R/W] H XXXXXXXX XXXXXXXX |  | BT5PDUT / BT5PRLH / BT5DTBF [R/W] H XXXXXXXX XXXXXXXX |  |  |
| 0000 0F5CH | - |  |  |  |  |
| 0000 0F60н | $\begin{gathered} \text { BT6TMR [R] H } \\ 0000000000000000 \end{gathered}$ |  |  |  | Base timer ch. 6 |
| 0000 0F64H | - | BT6STC [R/W] B $0000-000$ |  |  |  |
| 0000 0F68н | BT6PCSR / BT6PRLL [R/W] H XXXXXXXX XXXXXXXX |  | BT6PDUT / BT6PRLH / BT6DTBF [R/W] H XXXXXXXX XXXXXXXX |  |  |
| 0000 0F6CH | - |  |  |  |  |
| 0000 0F70н | $\begin{gathered} \text { BT7TMR [R] H } \\ 0000000000000000 \end{gathered}$ |  | BT7TMCR [R/W] B,H -0000000 00000000 |  | Base timer ch. 7 |
| 0000 0F74H | - | $\begin{gathered} \text { BT7STC [R/W] B } \\ 0000-000 \end{gathered}$ |  |  |  |
| 0000 0F78н | BT7PCSR / BT7PRLL [R/W] H XXXXXXXX XXXXXXXX |  | BT7PDUT / BT7PRLH / BT7DTBF [R/W] H XXXXXXXX XXXXXXXX |  |  |
| 0000 0F7CH | $\begin{gathered} \text { BTSEL4567 } \\ {[R / W] \text { B }} \\ 00000000 \end{gathered}$ |  | - |  |  |

(Continued)

## MB91625 Series

| Address | Register |  |  |  | Block |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 | +3 |  |
| 0000 0F80н | BT8TMR [R] H 0000000000000000 |  | $\begin{aligned} & \hline \text { BT8TMCR [R/W] B,H } \\ & -000000000000000 \end{aligned}$ |  | Base timer ch. 8 |
| 0000 0F84н | - | BT8STC [R/W] B $0000-000$ |  |  |  |
| 0000 0F88н | BT8PCSR / BT8PRLL [R/W] H XXXXXXXX XXXXXXXX |  | BT8PDUT / BT8PRLH / BT8DTBF [R/W] H XXXXXXXX XXXXXXXX |  |  |
| 0000 0F8CH | - |  |  |  |  |
| 0000 0F90н | BT9TMR [R] H 0000000000000000 |  |  |  | Base timer ch. 9 |
| 0000 0F94н | - | BT9STC [R/W] B $0000-000$ |  |  |  |
| 0000 0F98н | BT9PCSR / BT9PRLL [R/W] H XXXXXXXX XXXXXXXX |  | BT9PDUT / BT9PRLH / BT9DTBF [R/W] H <br> xxxxxxxx xxxxxxxx |  |  |
| 0000 OF9CH | - |  |  |  |  |
| 0000 OFAOH | BTATMR [R] H 0000000000000000 |  |  |  | Base timer ch. 10 |
| 0000 0FA4 | - | BTASTC [R/W] B $0000-000$ |  |  |  |
| 0000 0FA8н | BTAPCSR / BTAPRLL [R/W] H XXXXXXXX XXXXXXXX |  | BTAPDUT / BTAPRLH / BTADTBF [R/W] H XXXXXXXX XXXXXXXX |  |  |
| 0000 OFACH | - |  |  |  |  |
| 0000 0FB0н | BTBTMR [R] H 0000000000000000 |  | BTBTMCR [R/W] B,H -0000000 00000000 |  | Base timer ch. 11 |
| 0000 0FB4н | - | BTBSTC [R/W] B $0000-000$ |  |  |  |
| 0000 0FB8 | BTBPCSR / BTBPRLL [R/W] H XXXXXXXX XXXXXXXX |  | BTBPDUT / BTBPRLH / BTBDTBF [R/W] H xxxxxxxx xxxxxxxx |  |  |
| 0000 OFBCH | BTSEL89AB [R/W] B 00000000 |  | - |  |  |

(Continued)

## MB91625 Series

(Continued)

| Address | Register |  |  | Block |
| :---: | :---: | :---: | :---: | :---: |
|  | +0 | +1 | +2 |  |
| 0000 OFCOH | BTCTMR [R] H0000000000000000 |  | BTCTMCR [R/W] B,H $-000000000000000$ | Base timer ch. 12 |
| 0000 OFC4H | - | $\begin{gathered} \text { BTCSTC [R/W] B } \\ 0000-000 \end{gathered}$ |  |  |
| 0000 0FC8 | BTCPCSR / BTCPRLL [R/W] H XXXXXXXX XXXXXXXX |  | BTCPDUT / BTCPRLH / BTCDTBF [R/W] H XXXXXXXX XXXXXXXX |  |
| 0000 OFCCH | - |  |  |  |
| 0000 OFDOH | BTDTMR [R] H0000000000000000 |  |  | Base timer ch. 13 |
| 0000 0FD4 | - | $\begin{gathered} \text { BTDSTC [R/W] B } \\ 0000-000 \end{gathered}$ |  |  |
| 0000 0FD8н | BTDPCSR / BTDPRLL [R/W] H XXXXXXXX XXXXXXXX |  | BTDPDUT / BTDPRLH / BTDDTBF [R/W] H XXXXXXXX XXXXXXXX |  |
| 0000 OFDCH | - |  |  |  |
| 0000 OFEOH | $\begin{gathered} \text { BTETMR [R] H } \\ 0000000000000000 \end{gathered}$ |  |  | Base timer ch. 14 |
| 0000 OFE4H | - | $\begin{gathered} \text { BTESTC [R/W] B } \\ 0000-000 \end{gathered}$ |  |  |
| 0000 0FE8 ${ }^{\text {H }}$ | BTEPCSR / BTEPRLL [R/W] H XXXXXXXX XXXXXXXX |  | BTEPDUT / BTEPRLH / BTEDTBF [R/W] H XXXXXXXX XXXXXXXX |  |
| 0000 OFECH | - |  |  |  |
| 0000 OFFOH | BTFTMR [R] H0000000000000000 |  |  | Base timer ch. 15 |
| 0000 OFF4H | - | $\begin{gathered} \text { BTFSTC [R/W] B } \\ 0000-000 \end{gathered}$ |  |  |
| 0000 0FF8н | BTFPCSR / BTFPRLL [R/W] H XXXXXXXX XXXXXXXX |  | BTFPDUT / BTFPRLH / BTFDTBF [R/W] H XXXXXXXX XXXXXXXX |  |
| 0000 OFFCH | $\begin{gathered} \text { BTSELCDEF } \\ {[R / W] \text { B }} \\ 00000000 \end{gathered}$ | - |  |  |
| $\begin{gathered} 00001000 \text { н } \\ \text { to } \\ 000 \text { FFFCH } \end{gathered}$ |  | - |  | Reserved |

*1 : Byte access is available only when accessing the lower 8 bits within 9 bits.
*2 : The register of $\mathrm{I}^{2} \mathrm{C}$ can not be read immediate after reset.
*3 : Value just after reset by INIT pin.
Do not access the reserved areas.

## MB91625 Series

## VECTOR TABLE

| Interrupt source (Peripheral resource) | Interrupt number |  | Interrupt level setting register | Offset | Address of TBR default |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | Decimal | Hexadecimal |  |  |  |
| Reset | 0 | 00 | - | 3FCH | 000F FFFFCH |
| System reserved | 1 | 01 | - | 3F8H | 000F FFFF8 |
| System reserved | 2 | 02 | - | 3F4H | 000F FFFF4 |
| System reserved | 3 | 03 | - | 3F0H | 000F FFFFOH |
| System reserved | 4 | 04 | - | 3ЕСн | 000F FFECH |
| System reserved | 5 | 05 | - | 3Е8н | 000F FFE8н |
| System reserved | 6 | 06 | - | 3E4н | 000F FFE4н |
| System reserved | 7 | 07 | - | 3E0н | 000F FFE0н |
| System reserved | 8 | 08 | - | 3DCH | 000F FFDCH |
| INTE instruction | 9 | 09 | - | 3D8н | 000F FFD8н |
| System reserved | 10 | 0A | - | 3D4н | 000F FFD4н |
| System reserved | 11 | OB | - | 3D0н | 000F FFD0н |
| Step trace trap | 12 | OC | - | 3ССн | 000F FFCCH |
| System reserved | 13 | OD | - | 3C8H | 000F FFC8\% |
| Undefined instruction exception | 14 | OE | - | 3C4H | 000F FFCC4 |
| - | 15 | OF | 15(FH) fixed | 3С0н | 000F FFCOH |
| External interrupt request ch. 0 to ch. 7 | 16 | 10 | ICR00 | 3ВСн | 000F FFBCH |
| External interrupt request ch. 8 to ch. 15 | 17 | 11 | ICR01 | 3В8н | 000F FFB8н |
| External interrupt request ch. 16 to ch. 23 | 18 | 12 | ICR02 | 3В4н | 000F FFB4н |
| External interrupt request ch. 24 to ch. 31 | 19 | 13 | ICR03 | 3B0н | 000F FFB0н |
| 16-bit reload timer ch. 0 to ch. 2 | 20 | 14 | ICR04 | 3 ACH | 000F FFACH |
| Reception interrupt request of UART/CSIO ch. 0 | 21 | 15 | ICR05 | 3A8H | 000F FFA8н |
| Transmission interrupt request of UART/CSIO ch. 0 Transmission bus idle interrupt request of UART/CSIO ch. 0 | 22 | 16 | ICR06 | 3A4н | 000F FFA4н |
| Reception interrupt request of UART/CSIO/ I2 ${ }^{2}$ ch. 1 | 23 | 17 | ICR07 | 3A0н | 000F FFA0н |
| Transmission interrupt request of UART/CSIO/ I ${ }^{2} \mathrm{C}$ ch. 1 Transmission bus idle interrupt request of UART/CSIO ch. 1 | 24 | 18 | ICR08 | 39C | 000F FF9Cн |
| Status interrupt request of $\mathrm{I}^{2} \mathrm{C}$ ch. 1 | 25 | 19 | ICR09 | 398H | 000F FF98 ${ }^{\text {¢ }}$ |
| Reception interrupt request of UART/CSIO// ${ }^{2} \mathrm{C}$ ch. 2 | 26 | 1A | ICR10 | 394 ${ }^{\text {H }}$ | 000F FF94 ${ }^{\text {¢ }}$ |
| Transmission interrupt request of UART/CSIO/I²C ch.2 Transmission bus idle interrupt request of UART/CSIO ch. 2 | 27 | 1B | ICR11 | 390н | 000F FF90н |

(Continued)

## MB91625 Series

| Interrupt source (Peripheral resource) | Interrupt number |  | Interrupt level setting register | Offset | Address of TBR default |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | Decimal | Hexadecimal |  |  |  |
| Status interrupt request of ${ }^{2} \mathrm{C}$ ch. 2 | 28 | 1C | ICR12 | 38CH | 000F FF8CH |
| Reception interrupt request of UART/CSIO/I² ${ }^{\text {C }}$ ch. 3 | 29 | 1D | ICR13 | 388H | 000F FF88н |
| Transmission interrupt request of UART/CSIO//² C ch. 3 Transmission bus idle interrupt request of UART/ CSIO ch. 3 Status interrupt request of $I^{2} \mathrm{C}$ ch. 3 | 30 | 1E | ICR14 | 384H | 000F FF84н |
| Reception interrupt request of UART/CSIO/I² ${ }^{\text {C }}$ ch. 4 | 31 | 1F | ICR15 | 380 ${ }^{\text {H}}$ | 000F FF80н |
| Transmission interrupt request of UART/CSIO//²C ch. 4 Transmission bus idle interrupt request of UART/ CSIO ch. 4 Status interrupt request of $\mathrm{I}^{2} \mathrm{C}$ ch. 4 | 32 | 20 | ICR16 | $37 \mathrm{CH}_{4}$ | 000F FF7CH |
| Reception interrupt request of UART/CSIO/I ${ }^{2} \mathrm{C}$ ch. 5 | 33 | 21 | ICR17 | 378H | 000F FF78H |
| Transmission interrupt request of UART/CSIO/I² C ch. 5 Transmission bus idle interrupt request of UART/ CSIO ch. 5 Status interrupt request of $\mathrm{I}^{2} \mathrm{C}$ ch. 5 | 34 | 22 | ICR18 | 374H | 000F FF74H |
| Reception interrupt request of UART/CSIO/ ${ }^{2} \mathrm{C}$ ch. 6 | 35 | 23 | ICR19 | 370 ${ }^{\text {H}}$ | 000F FF70н |
| Transmission interrupt request of UART/CSIO// ${ }^{2} \mathrm{C}$ ch. 6 Transmission bus idle interrupt request of UART/ CSIO ch. 6 Status interrupt request of $\mathrm{I}^{2} \mathrm{C}$ ch. 6 | 36 | 24 | ICR20 | $36 \mathrm{CH}_{\mathrm{H}}$ | 000F FF6CH |
| Reception interrupt request of UART/CSIO/I² C ch. 7 32-bit input capture ch. 4 to ch. 7 | 37 | 25 | ICR21 | 368H | 000F FF68н |
| Transmission interrupt request of UART/CSIO//² C ch. 7 Transmission bus idle interrupt request of UART/ CSIO ch. 7 Status interrupt request of ${ }^{2} \mathrm{C}$ ch. 7 32-bit output compare ch. 4 to ch. 7 | 38 | 26 | ICR22 | 364H | 000F FF64H |
| Reception interrupt request of UART/CSIO/I2 C ch. 8 to ch. 11 Transmission interrupt request of UART/CSIO/ ${ }^{2} \mathrm{C}$ ch. 8 to ch. 11 Transmission bus idle interrupt request of UART/CSIO ch. 8 to ch. 11 Transmission FIFO interrupt request UART/CSIO/I² Ch .8 to ch. 11 Status interrupt request of $I^{2} \mathrm{C}$ ch. 8 to ch. 11 | 39 | 27 | ICR23 | 360 ${ }^{\text {H}}$ | 000F FF60н |
| 16-bit up/down counter ch. 0 to ch. 3 | 40 | 28 | ICR24 | $35 \mathrm{CH}_{\mathrm{H}}$ | 000F FF5CH |
| Main timer/Sub timer/Watch counter | 41 | 29 | ICR25 | 358H | 000F FF58н |
| Unit 0 of 10 -bit A/D converter <br> - Scan conversion interrupt request <br> - Priority conversion interrupt request <br> - FIFO overrun interrupt request <br> - Conversion result compare interrupt request | 42 | 2 A | ICR26 | 354 | 000F FF54н |
| 32-bit free run timer ch.0, ch. 1 | 43 | 2B | ICR27 | 350H | 000F FF50h |
| 32-bit input capture ch. 0 to ch. 3 | 44 | 2C | ICR28 | 34 CH | 000F FF4CH |
| 32-bit output compare ch. 0 to ch. 3 | 45 | 2D | ICR29 | 348н | 000F FF48н |

(Continued)

## MB91625 Series

(Continued)

| Interrupt source (Peripheral resource) | Interrupt number |  | Interrupt level setting register | Offset | Address of TBR default |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  | Decimal | Hexadecimal |  |  |  |
| Base timer ch. 0 | 46 | 2E | ICR30 | 344 | 000F FF44 |
| Base timer ch. 1 | 47 | 2F | ICR31 | 340н | 000F FF40н |
| Base timer ch. 2 | 48 | 30 | ICR32 | 33С | 000F FF3CH |
| Base timer ch. 3 | 49 | 31 | ICR33 | 338н | 000F FF38 |
| Base timer ch.4, ch. 5 | 50 | 32 | ICR34 | 334н | 000F FF34 |
| Base timer ch.6, ch. 7 | 51 | 33 | ICR35 | 330н | 000F FF30н |
| Base timer ch.8, ch. 9 | 52 | 34 | ICR36 | 32 CH | 000F FF2CH |
| Base timer ch.10, ch. 11 | 53 | 35 | ICR37 | 328н | 000F FF28 |
| Base timer ch. 12 | 54 | 36 | ICR38 | 324н | 000F FF24H |
| Base timer ch. 13 | 55 | 37 | ICR39 | 320н | 000F FF20н |
| Base timer ch.14, ch. 15 | 56 | 38 | ICR40 | $31 \mathrm{CH}^{\text {¢ }}$ | 000F FF1CH |
| DMA controller (DMAC) ch. 0 | 57 | 39 | ICR41 | 318H | 000F FF18 |
| DMA controller (DMAC) ch. 1 | 58 | 3A | ICR42 | 314н | 000F FF14H |
| DMA controller (DMAC) ch. 2 | 59 | 3B | ICR43 | 310н | 000F FF10н |
| DMA controller (DMAC) ch. 3 | 60 | 3C | ICR44 | 30 CH | 000F FFOCH |
| DMA controller (DMAC) ch. 4 to ch. 7 | 61 | 3D | ICR45 | 308н | 000F FF08н |
| System reserved | 62 | 3E | ICR46 | 304н | 000F FF04H |
| Delay interrupt | 63 | 3 F | ICR47 | 300н | 000F FFOOH |
| System reserved (Used by REALOS) | 64 | 40 | - | 2 FCH | 000F FEFCH |
| System reserved (Used by REALOS) | 65 | 41 | - | 2F8H | 000F FEF8H |
| Used by INT instruction | $\begin{array}{r} 66 \\ \text { to } \\ 255 \end{array}$ | $\begin{array}{r} 42 \\ \text { to } \\ \text { FF } \end{array}$ | - | $\begin{gathered} 2 F 4 \mathrm{H} \\ \text { to } \\ 00 \mathrm{O}_{\mathrm{H}} \end{gathered}$ | $\begin{aligned} & \text { O00F FEF4н } \\ & \text { to } \\ & 000 \mathrm{FCO} \end{aligned}$ |

## MB91625 Series

## PIN STATUS IN EACH CPU STATE

The terms used for pin status have the following meanings.

- When INIT = "L"

This is the period when the INIT pin is the "L" level.

- When $\overline{\mathrm{N} I \mathrm{~T}}=$ " H "

The status immediately after the INIT pin changes from the " L " level to the " H " level.

- SLVL1

This bit is a standby level setting bit in the standby mode control register (STBCR).

- Input enabled

Indicates that the input function can be used.

- Input disabled

Indicates that the input function cannot be used.

- Output Hi-Z

Indicates that the output drive transistor is disabled and the pin is put in the $\mathrm{Hi}-\mathrm{Z}$ state.

- Maintain previous state

Maintains the state that was being output immediately prior to entering the current mode.
If a built-in peripheral function is operating, the output follows the peripheral function.
If the pin is being used as a port, that output is maintained.

- Internal input fixed at " 0 "

The input gate connected to the pin is disconnected from the external input and internally connected to " 0 ".

- Input enabled when interrupt function selected and enabled

Inputs are allowed only when the pin is configured as an external interrupt request input pin and the external interrupt request is enabled.

## MB91625 Series

- List of pin status

| Pin name | Function name | Initial Value |  | Sleep Mode | Standby Mode |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{gathered} \hline \text { INIT }=\text { "L" } \\ \text { Period } \end{gathered}$ | $\begin{gathered} \text { INIT }=\text { "H" } \\ \text { Period } \end{gathered}$ |  | SLVL1 $=0$ | SLVL1 = 1 |
| INIT | INIT | - | - | Input enabled | Input enabled | Input enabled |
| X0 | X0 | Input enabled | Input enabled |  | Hi-Z or Input enabled | Hi-Z or Input enabled |
| X1 | X1 | Input enabled | Input enabled |  | "H" output or Input enabled | "H" output or Input enabled |
| X0A | XOA (When $\overline{\text { INIT }}$ input, see PK1. When port selected, input disabled) | Input disabled | Input disabled |  | Hi-Z or Input enabled | Hi-Z or Input enabled |
| X1A | X1A (When INIT input, see PK0. When port selected, input disabled) | Input disabled | Input disabled |  | "H" output or Input enabled | "H" output or Input enabled |
| MD0 | MD0 | Input enabled | Input enabled |  | Input | Inp |
| MD1 | MD1 | Input enabled | Input enabled |  | enabled | enabled |
| P00 | P00/TIOA0/SOUTO_1/INO | Output Hi-Z | Output Hi-Z/Input enabled | Last state maintained | Last state maintained | Output Hi-Z/ Internal input " 0 " fixed |
| P01 | P01/TIOB0/SIN0_1/IN1 |  |  |  |  |  |
| P02 | P02/TIOA1/SCK0_1/IN2 |  |  |  |  |  |
| P03 | P03/TIOB1/IN3 |  |  |  |  |  |
| P04 | P04/TIOA2/SOUT1/IN4 |  |  |  |  |  |
| P05 | P05/TIOB2/SIN1/IN5 |  |  |  |  |  |
| P06 | P06/TIOA3/SCK1/IN6 |  |  |  |  |  |
| P07 | P07/TIOB3/IN7 |  |  |  |  |  |
| P10 | P10/TIOA4/SOUT2/AIN0/INT0 | Output Hi-Z | Output Hi-Z/Input enabled | Last state maintained | Last state maintained | Output Hi-Z/ Internal input "0" fixed Input enabled when the selection of interruptfunction is enabled |
| P11 | P11/TIOB4/SIN2/BIN0/INT1 |  |  |  |  |  |
| P12 | P12/TIOA5/SCK2/ZIN0/INT2 |  |  |  |  |  |
| P13 | P13/TIOB5/INT3 |  |  |  |  |  |
| P14 | P14/TIOA6/SOUT3/AIN1/INT4 |  |  |  |  |  |
| P15 | P15/TIOB6/SIN3/BIN1/INT5 |  |  |  |  |  |
| P16 | P16/TIOA7/SCK3/ZIN1/INT6 |  |  |  |  |  |
| P17 | P17/TIOB7/INT7 |  |  |  |  |  |

(Continued)

## MB91625 Series

|  | Function name | Initial Value |  | Sleep Mode | Standby Mode |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| name |  | $\begin{gathered} \hline \overline{\text { INIT }}=\text { "L" } \\ \text { Period } \end{gathered}$ | $\begin{gathered} \overline{\mathrm{INIT}}=\text { "H" } \\ \text { Period } \end{gathered}$ |  | SLVL1 $=0$ | SLVL1 $=1$ |
| P20 | P20/TIOA8/SOUT4/AIN2 | Output Hi-Z | Output Hi-Z/Input enabled | Last state maintained | Last state maintained | Output Hi -Z/Internal input "0" fixed |
| P21 | P21/TIOB8/SIN4/BIN2 |  |  |  |  |  |
| P22 | P22/TIOA9/SCK4/ZIN2 |  |  |  |  |  |
| P23 | P23/TIOB9 |  |  |  |  |  |
| P24 | P24/TIOA10/SOUT5/AIN3/OUT0 |  |  |  |  |  |
| P25 | P25/TIOB10/SIN5/BIN3/OUT1 |  |  |  |  |  |
| P26 | P26/TIOA11/SCK5/ZIN3/OUT2 |  |  |  |  |  |
| P27 | P27/TIOB11/OUT3 |  |  |  |  |  |
| P30 | P30/TIOA12/SOUT6/INT8 | Output Hi-Z | Output <br> Hi-Z/Input enabled | Last state maintained | Last state maintained | Output <br> Hi-Z/Internal input "0" fixed <br> Input enabled when the selection of interrupt function is enabled |
| P31 | P31/TIOB12/SIN6/INT9 |  |  |  |  |  |
| P32 | P32/TIOA13/SCK6/INT10 |  |  |  |  |  |
| P33 | P33/TIOB13/INT11 |  |  |  |  |  |
| P34 | P34/TIOA14/SOUT7/OUT4/ INT12 |  |  |  |  |  |
| P35 | P35/TIOB14/SIN7/OUT5/INT13 |  |  |  |  |  |
| P36 | P36/TIOA15/SCK7/OUT6/INT14 |  |  |  |  |  |
| P37 | P37/TIOB15/OUT7/INT15 |  |  |  |  |  |
| P40 | P40/SOUT8 | Output Hi-Z | Output Hi-Z/Input enabled | Last state maintained | Last state maintained | Output Hi-Z/Internal input "0" fixed |
| P41 | P41/SIN8 |  |  |  |  |  |
| P42 | P42/SCK8 |  |  |  |  |  |
| P43 | P43 |  |  |  |  |  |
| P44 | P44/SOUT9 |  |  |  |  |  |
| P45 | P45/SIN9 |  |  |  |  |  |
| P46 | P46/SCK9 |  |  |  |  |  |
| P47 | P47 |  |  |  |  |  |

(Continued)

## MB91625 Series


(Continued)

## MB91625 Series

| Pin name | Function name | Initial Value |  | Sleep Mode | Standby Mode |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\begin{aligned} & \hline \overline{\text { INIT }}=\text { "L" } \\ & \text { Period } \end{aligned}$ | $\begin{gathered} \overline{\mathrm{INIT}}=\text { "H" } \\ \text { Period } \end{gathered}$ |  | SLVL1 $=0$ | SLVL1 $=1$ |
| P60 | P60/AIN2_1 | Output Hi-Z | Output HiZ/Input enabled | Last state maintained or Input enabled | Last state maintained | Output Hi-Z/ Internal input "0" fixed |
| P61 | P61/BIN2_1 |  |  |  |  |  |
| P62 | P62/ZIN2_1 |  |  |  |  |  |
| P63 | P63/FRCK1_1/INT22_2 |  |  |  |  | Output Hi-Z/ Internal input "0" fixed Input enabled when the selection of interrupt function is enabled |
| P64 | P64/AIN3_1 |  |  |  |  |  |
| P65 | P65/BIN3_1/ADTRG0_1 |  |  |  |  | Output Hi-Z/ Internal input "0" fixed |
| P66 | P66/ZIN3_1/FRCK0_1 |  |  |  |  |  |
| P67 | P67/INT23_2 |  |  |  |  | Output Hi-Z/ Internal input "0" fixed Input enabled when the selection of interrupt function is enabled |
| P70 | P70/AN0/OUT0_1/INT16 | Output Hi-Z | Output Hi-Z/Input disabled | Last state maintained | Last state maintained | Output Hi-Z/ Internal input "0" fixed Input enabled when the selection of interrupt function is enabled |
| P71 | P71/AN1/OUT1_1/INT17 |  |  |  |  |  |
| P72 | P72/AN2/TMO0/OUT2_1/INT18 |  |  |  |  |  |
| P73 | P73/AN3/TMO1/OUT3_1/INT19 |  |  |  |  |  |
| P74 | P74/AN4/TMO2/OUT4_1/INT20 |  |  |  |  |  |
| P75 | P75/AN5/SOUT0/TMIO/OUT5_1/ INT21 |  |  |  |  |  |
| P76 | P76/AN6/SIN0/TMII/OUT6_1/ <br> INT22 |  |  |  |  |  |
| P77 | P77/AN7/SCK0/TMI2/OUT7_1/ INT23 |  |  |  |  |  |

(Continued)

## MB91625 Series

(Continued)

|  | Function name | Initial Value |  | Sleep Mode | Standby Mode |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| name |  | $\begin{gathered} \hline \overline{\text { INITT }}=\text { "L" } \\ \text { Period } \end{gathered}$ | $\begin{aligned} & \hline \overline{\text { NITT }}=\text { "H" } \\ & \text { Period } \end{aligned}$ |  | SLVL1 $=0$ | SLVL1 $=1$ |
| P80 | P80/AN8/IN0_1/INT24 | Output Hi-Z | Output Hi-Z/Input disabled | Last state maintained | Last state maintained | Output Hi-Z/ <br> Internal input "0" <br> fixed <br> Input <br> enabled when the selection of interrupt function is enabled |
| P81 | P81/AN9/IN1_1/INT25 |  |  |  |  |  |
| P82 | P82/AN10/IN2_1/INT26 |  |  |  |  |  |
| P83 | P83/AN11/IN3_1/INT27 |  |  |  |  |  |
| P84 | P84/AN12/IN4_1/INT28 |  |  |  |  |  |
| P85 | P85/AN13/IN5_1/INT29 |  |  |  |  |  |
| P86 | P86/AN14/IN6_1/INT30 |  |  |  |  |  |
| P87 | P87/AN15/IN7_1/INT31 |  |  |  |  |  |
| P90 | P90/DA0 | Output Hi-Z | Output Hi-Z/Input enabled | Last state maintained | Last state maintained | Output Hi-Z/ Internal input "0" fixed |
| P91 | P91/DA1 |  |  |  |  |  |
| P92 | P92 |  |  |  |  |  |
| PA0 | PA0/INT16_1 | Output Hi-Z | Output <br> Hi-Z/Input disabled | Last state maintained | Last state maintained | Output Hi-Z/ <br> Internal input "0" fixed <br> Input <br> enabled when the selection of interrupt function is enabled |
| PA1 | PA1/INT17_1 |  |  |  |  |  |
| PA2 | PA2/TMO0_1/INT18_1 |  |  |  |  |  |
| PA3 | PA3/TMO1_1/INT19_1 |  |  |  |  |  |
| PA4 | PA4/TMO2_1/INT20_1 |  |  |  |  |  |
| PA5 | PA5/TMIO_1/INT21_1 |  |  |  |  |  |
| PA6 | PA6/TMI1_1/INT22_1 |  |  |  |  |  |
| PA7 | PA7/TMI2_1/INT23_1 |  |  |  |  |  |
| PK0 | PKO | Output Hi-Z | Internal input "0" fixed | Last state maintained | Last state maintained | Output $\mathrm{Hi}-\mathrm{Z} /$ Internal input "0" fixed |
| PK1 | PK1 |  | Output |  |  |  |
| PK2 | PK2/ADTRG0_2 |  | put enabled |  |  |  |

## MB91625 Series

- List of pin status (serial write mode)

| Pin name | Function name | During initialization | During asynchronous write operation | During synchronous write operation |
| :---: | :---: | :---: | :---: | :---: |
|  |  | $\overline{\text { INIT }}=$ "L" | $\overline{\text { INTT }}=$ " ${ }^{\text {H" }}$ |  |
| $\overline{\mathrm{INIT}}$ | $\overline{\text { INIT }}$ | - | - | - |
| X0 | X0 | Input enabled | Input enabled | Input enabled |
| X1 | X1 | Input enabled | Input enabled | Input enabled |
| X0A | XOA (When INIT input, see PK1. When port selected, input disabled) | Input disabled | Input disabled | Input disabled |
| X1A | X1A (When INIT input, see PK0. When port selected, input disabled) | Input disabled | Input disabled | Input disabled |
| MD0 | MD0 | Input enabled | Input enabled | Input enabled |
| MD1 | MD1 | Input enabled | Input enabled | Input enabled |
| P00 | P00/TIOAO/SOUTO_1/INO | Output Hi-Z | Output <br> Hi-Z/Input enabled | Output Hi-Z/Input enabled |
| P01 | P01/TIOB0/SIN0_1/IN1 |  |  |  |
| P02 | P02/TIOA1/SCK0_1/IN2 |  |  |  |
| P03 | P03/TIOB1/IN3 |  |  |  |
| P04 | P04/TIOA2/SOUT1/IN4 |  |  |  |
| P05 | P05/TIOB2/SIN1/IN5 |  |  |  |
| P06 | P06/TIOA3/SCK1/IN6 |  |  |  |
| P07 | P07/TIOB3/IN7 |  |  |  |
| P10 | P10/TIOA4/SOUT2/AIN0/INT0 | Output Hi-Z | Output <br> Hi-Z/Input enabled | Output Hi-Z/Input enabled |
| P11 | P11/TIOB4/SIN2/BIN0/INT1 |  |  |  |
| P12 | P12/TIOA5/SCK2/ZIN0/INT2 |  |  |  |
| P13 | P13/TIOB5/INT3 |  |  |  |
| P14 | P14/TIOA6/SOUT3/AIN1/INT4 |  |  |  |
| P15 | P15/TIOB6/SIN3/BIN1/INT5 |  |  |  |
| P16 | P16/TIOA7/SCK3/ZIN1/INT6 |  |  |  |
| P17 | P17/TIOB7/INT7 |  |  |  |

(Continued)

## MB91625 Series

| Pin name | Function name | During initialization | During asynchronous write operation | During synchronous write operation |
| :---: | :---: | :---: | :---: | :---: |
|  |  | $\overline{\text { INIT }}$ = "L" | $\overline{\text { INIT }}$ = "H" |  |
| P20 | P20/TIOA8/SOUT4/AIN2 | Output Hi-Z | Output Hi-Z/Input enabled | Output Hi-Z/Input enabled |
| P21 | P21/TIOB8/SIN4/BIN2 |  |  |  |
| P22 | P22/TIOA9/SCK4/ZIN2 |  |  |  |
| P23 | P23/TIOB9 |  |  |  |
| P24 | P24/TIOA10/SOUT5/AIN3/OUT0 |  |  |  |
| P25 | P25/TIOB10/SIN5/BIN3/OUT1 |  |  |  |
| P26 | P26/TIOA11/SCK5/ZIN3/OUT2 |  |  |  |
| P27 | P27/TIOB11/OUT3 |  |  |  |
| P30 | P30/TIOA12/SOUT6/INT8 | Output Hi-Z | Output <br> Hi-Z/Input enabled | Output Hi-Z/Input enabled |
| P31 | P31/TIOB12/SIN6/INT9 |  |  |  |
| P32 | P32/TIOA13/SCK6/INT10 |  |  |  |
| P33 | P33/TIOB13/INT11 |  |  |  |
| P34 | P34/TIOA14/SOUT7/OUT4/ INT12 |  |  |  |
| P35 | P35/TIOB14/SIN7/OUT5/INT13 |  |  |  |
| P36 | P36/TIOA15/SCK7/OUT6/INT14 |  |  |  |
| P37 | P37/TIOB15/OUT7/INT15 |  |  |  |
| P40 | P40/SOUT8 | Output Hi-Z | Output Hi-Z/Input enabled | Output Hi-Z/Input enabled |
| P41 | P41/SIN8 |  |  |  |
| P42 | P42/SCK8 |  |  |  |
| P43 | P43 |  |  |  |
| P44 | P44/SOUT9 |  |  |  |
| P45 | P45/SIN9 |  |  |  |
| P46 | P46/SCK9 |  |  |  |
| P47 | P47 |  |  |  |
| P50 | P50/SOUT10/AIN0_1 | Output Hi-Z | Output Hi-Z/Input enabled | Output <br> Hi-Z/Input enabled |
| P51 | P51/SIN10/BIN0_1 |  |  |  |
| P52 | P52/SCK10/ZIN0_1 |  |  |  |
| P53 | P53/FRCK1/INT21_2 |  |  |  |
| P54 | P54/SOUT11/AIN1_1 |  |  |  |
| P55 | P55/SIN11/BIN1_1/ADTRG0 |  |  |  |
| P56 | P56/SCK11/ZIN1_1/FRCK0 |  |  |  |
| P57 | P57 |  |  |  |

(Continued)

## MB91625 Series

| Pin name | Function name | During initialization | During asynchronous write operation | During synchronous write operation |
| :---: | :---: | :---: | :---: | :---: |
|  |  | $\overline{\text { INIT }=\text { "L" }}$ | $\overline{\text { INIT }=\text { "H" }}$ |  |
| P60 | P60/AIN2_1 | Output Hi-Z | Output Hi-Z/Input enabled | Output Hi-Z/Input enabled |
| P61 | P61/BIN2_1 |  |  |  |
| P62 | P62/ZIN2_1 |  |  |  |
| P63 | P63/FRCK1_1/INT22_2 |  |  |  |
| P64 | P64/AIN3_1 |  |  |  |
| P65 | P65/BIN3_1/ADTRG0_1 |  |  |  |
| P66 | P66/ZIN3_1/FRCK0_1 |  |  |  |
| P67 | P67/INT23_2 |  |  |  |
| P70 | P70/AN0/OUT0_1/INT16 | Output Hi-Z | Output Hi-Z/Input disabled | Output Hi-Z/Input disabled |
| P71 | P71/AN1/OUT1_1/INT17 |  |  |  |
| P72 | P72/AN2/TMO0/OUT2_1/INT18 |  |  |  |
| P73 | P73/AN3/TMO1/OUT3_1/INT19 |  |  |  |
| P74 | P74/AN4/TMO2/OUT4_1/INT20 |  |  |  |
| P75 | P75/AN5/SOUT0/TMI0/OUT5_1/ <br> INT21 | Output Hi-Z/Input enabled | Output | Output |
| P76 | P76/AN6/SIN0/TMI1/OUT6_1/ INT22 | Output Hi-Z | Output Hi-Z/ Input enabled | Output Hi-Z/ Input enabled |
| P77 | P77/AN7/SCK0/TMI2/OUT7_1/ INT23 |  | Output Hi-Z/ Input disabled | Output Hi-Z/ Input disabled |
| P80 | P80/AN8/IN0_1/INT24 | Output Hi-Z | Output Hi-Z/Input disabled | Output Hi-Z/Input disabled |
| P81 | P81/AN9/IN1_1/INT25 |  |  |  |
| P82 | P82/AN10/IN2_1/INT26 |  |  |  |
| P83 | P83/AN11/IN3_1/INT27 |  |  |  |
| P84 | P84/AN12/IN4_1/INT28 |  |  |  |
| P85 | P85/AN13/IN5_1/INT29 |  |  |  |
| P86 | P86/AN14/IN6_1/INT30 |  |  |  |
| P87 | P87/AN15/IN7_1/INT31 |  |  |  |
| P90 | P90/DA0 | Output Hi-Z | Output Hi-Z/Input enabled | Output Hi-Z/Input enabled |
| P91 | P91/DA1 |  |  |  |
| P92 | P92 |  |  |  |

(Continued)

## MB91625 Series

(Continued)

| Pin name | Function name | During initialization | During asynchronous write operation | During synchronous write operation |
| :---: | :---: | :---: | :---: | :---: |
|  |  | $\overline{\text { INIT }}$ = "L" | INIT = "H" |  |
| PA0 | PA0/INT16_1 | Output Hi-Z | Output <br> Hi-Z/Input disabled | Output <br> Hi-Z/Input disabled |
| PA1 | PA1/INT17_1 |  |  |  |
| PA2 | PA2/TMO0_1/INT18_1 |  |  |  |
| PA3 | PA3/TMO1_1/INT19_1 |  |  |  |
| PA4 | PA4/TMO2_1/INT20_1 |  |  |  |
| PA5 | PA5/TMIO_1/INT21_1 |  |  |  |
| PA6 | PA6/TMI1_1/INT22_1 |  |  |  |
| PA7 | PA7/TMI2_1/INT23_1 |  |  |  |
| PK0 | PK0 | Output Hi-Z | Output Hi-Z/Input disabled | Output Hi-Z/Input disabled |
| PK1 | PK1 |  |  |  |
| PK2 | PK2/ADTRG0_2 |  | Output Hi-Z/Input enabled | Output <br> Hi-Z/Input enabled |

## MB91625 Series

## ■ ELECTRICAL CHARACTERISTICS

## 1. Absolute Maximum Ratings

| Parameter | Symbol | Rating |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Max |  |  |
| Power supply voltage*1, *2 | Vcc | Vss - 0.3 | Vss + 4.0 | V |  |
| Analog power supply voltage*1, *3 | AVcc | Vss -0.3 | Vss + 4.0 | V |  |
| Analog reference voltage*1, *3 | AVRH | Vss - 0.3 | Vss +4.0 | V |  |
| Input voltage*1 | V | Vss - 0.3 | $\mathrm{Vcc}+0.3(\leq 4.0)$ | V | *7 |
|  |  | Vss - 0.3 | Vss + 6.0 | V | 5 V tolerant |
| Analog pin input voltage*1 | VIA | Vss - 0.3 | Vss + 4.0 | V |  |
| Output voltage*1 | Vo | Vss - 0.3 | $\mathrm{Vcc}+0.3$ | V |  |
| Maximum clamp current | Iclamp | -4 | + 4 | mA | *8 |
| Total maximum clamp current | $\Sigma \mid$ Iclamp\| | - | 40 | mA | *8 |
| "L" level maximum output current*4 | loL | - | 10 | mA |  |
| "L" level average output current*5 | lolav | - | 4 | mA |  |
| "L" level total maximum output current | Elo | - | 100 | mA |  |
| "L" level total average output current* ${ }^{*}$ | Elolav | - | 50 | mA |  |
| "H" level maximum output current*4 | Іон | - | - 10 | mA |  |
| "H" level average output current*5 | lohav | - | -4 | mA |  |
| "H" level total maximum output current | Elon | - | - 100 | mA |  |
| "H" level total average output current* | $\Sigma$ Iohav | - | -50 | mA |  |
| Power consumption | PD | - | 500 | mW |  |
| Operating temperature | Ta | -40 | + 85 | ${ }^{\circ} \mathrm{C}$ |  |
| Storage temperature | Tsta | -55 | + 125 | ${ }^{\circ} \mathrm{C}$ |  |

*1: The parameter is based on $\mathrm{V}_{\mathrm{ss}}=\mathrm{AV} \mathrm{Vs}=0.0 \mathrm{~V}$.
*2 : Vcc must not drop below Vss - 0.3 V.
*3 : Be careful not to exceed $\mathrm{Vcc}+0.3 \mathrm{~V}$, for example, when the power is turned on.
*4 : The maximum output current is the peak value for a single pin.
*5 : The average output is the average current for a single pin over a period of 100 ms .
*6 : The total average output current is the average current for all pins over a period of 100 ms .
*7 : If the input current or the maximum input current are limited by some means with external components, the Iclamp rating supersedes the $\mathrm{V}_{1}$ rating.
(Continued)

## MB91625 Series

## 2. Recommended Operating Conditions

$$
\left(\mathrm{V}_{\mathrm{ss}}=\mathrm{AV} \mathrm{ss}=0.0 \mathrm{~V}\right)
$$

| Parameter | Symbol | Value |  | Unit | Remarks |
| :--- | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathrm{V}_{\mathrm{cc}}$ | 2.7 |  |  |
|  |  |  |  |  |  |
| Power supply voltage | AV cc | 2.7 | 3.6 | V | $\mathrm{AV} \mathrm{cc} \leq \mathrm{V}_{\mathrm{cc}}$ |
| Analog power supply voltage | AVRH | $\mathrm{AV}_{\mathrm{ss}}$ | $\mathrm{AV}_{\mathrm{cc}}$ | V |  |
| Analog reference voltage | Ta | -40 | +85 | ${ }^{\circ} \mathrm{C}$ |  |
| Operating temperature |  |  |  |  |  |

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.
Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

## MB91625 Series

(Continued)
$\left(\mathrm{V} \mathrm{cc}=\mathrm{AV} \mathrm{cc}=2.7 \mathrm{~V}\right.$ to 3.6 V , V ss $=\mathrm{AV} \mathrm{ss}=0 \mathrm{~V}, \mathrm{Ta}=-40^{\circ} \mathrm{C}$ to $\left.+85^{\circ} \mathrm{C}\right)$

| Parameter | $\begin{gathered} \text { Sym- } \\ \text { bol } \end{gathered}$ | Pin name | Conditions | Value |  |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max |  |  |
| "H" level output voltage | Vон | P00 to P07, <br> P10 to P17, <br> P20 to P27, <br> P30 to P37, <br> P40 to P47, <br> P50 to P57, <br> P60 to P67, <br> P70 to P77, | $\begin{gathered} \mathrm{V}_{\mathrm{cc}}=2.7 \mathrm{~V} \\ \mathrm{I} \mathrm{H}=-4 \mathrm{~mA} \end{gathered}$ | V cc-0.5 | - | Vcc | V |  |
| "L" level output voltage | VoL | P90 to P92, PA0 to PA7, PK0 to PK2 | $\begin{aligned} & \mathrm{V} \mathrm{cc}=2.7 \mathrm{~V} \\ & \mathrm{loL}=4 \mathrm{~mA} \end{aligned}$ | Vss | - | 0.4 | V |  |
|  |  |  |  | -5 | - | +5 | $\mu \mathrm{A}$ | Digital pin |
|  | 11. | - | - | - 10 | - | + 10 | $\mu \mathrm{A}$ | Analog pin |
| Pull-up resistance value | Rpu | Pull-up pin | - | 16.6 | 33 | 66 | $\mathrm{k} \Omega$ |  |
| Input capacitance | Cin | Other than Vcc, Vss, AVcc, AVss, AVRH | - | - | 10 | 15 | pF |  |

*1: When opened, all ports are fixed to output
*2 : $\mathrm{Ta}=+25^{\circ} \mathrm{C}$ and $\mathrm{Vcc}=3.3 \mathrm{~V}$
*3: X0 $=15 \mathrm{MHz}, \mathrm{CPU}$ clock $=60 \mathrm{MHz}$ and $\mathrm{XOA}=$ when stopped
*4 : X0 = STOP and XOA $=32 \mathrm{kHz}$

## - V -I characteristics

Conditions
Min : Process = Slow, $\mathrm{Ta}=+85^{\circ} \mathrm{C}, \mathrm{V} \mathrm{Cc}=2.7 \mathrm{~V}$
Typ : Process $=$ Typical, $\mathrm{Ta}=+25^{\circ} \mathrm{C}, \mathrm{V} \mathrm{cc}=3.3 \mathrm{~V}$
Max : Process $=$ Fast, $\mathrm{Ta}=-40^{\circ} \mathrm{C}, \mathrm{Vcc}=3.6 \mathrm{~V}$


Voh-Vcc [V]

Vol - Iol


## MB91625 Series

## - Operation guaranteed range

- When the main clock is selected ( $\mathrm{DIVB}=000$ )

- When the PLL clock is selected

*1 : DIVB $=111$, ODS $=11$, and PLL macro oscillation frequency $=30 \mathrm{MHz}$
*2 : DIVB $=000$, ODS $=01$, and PLL macro oscillation frequency $=60 \mathrm{MHz}$
- When the sub clock is selected ( $\mathrm{FcL}=32.768 \mathrm{kHz}$ )


Internal operation clock Fcc (kHz)

## MB91625 Series

- Example of configuration
- When the main clock is selected (DIVB $=000^{* 1}$ )
Internal operation clock
Fcc (MHz)

X0 input frequency (MHz)
- When the PLL clock is selected (DIVB $=000^{* 1}$, PDS $=0000^{* 2}$ )

- When the PLL clock is selected (DIVB $=000^{* 1}$, PDS $=0001^{* 2}$ )

*1 : The values other than DIVB $=000$ are omitted.
*2 : The values other than PDS = 0000 and 0001 are omitted.
Note: DIVB :Base clock division configuration bit
ODS :PLL macro oscillation clock division rate select bit
PDS :PLL input clock division select bit
PMS :PLL clock multiple rate select bit


## MB91625 Series

(2) Sub Clock (SBCLK) Input Standard
$\left(\mathrm{V} \mathrm{cc}=\mathrm{AV} \mathrm{cc}=2.7 \mathrm{~V}\right.$ to $3.6 \mathrm{~V}, \mathrm{~V}_{\mathrm{ss}}=\mathrm{AV} \mathrm{ss}=0 \mathrm{~V}, \mathrm{Ta}=-40^{\circ} \mathrm{C}$ to $\left.+85^{\circ} \mathrm{C}\right)$

| Parameter | Symbol | Pin name | Conditions | Value |  |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Typ | Max |  |  |
| Input frequency | Fcı | X0A, X1A | - | - | 32.768 | - | kHz | When crystal oscillator is connected |
|  |  |  | - | - | 32.768 | - | kHz | When using external clock |
| Input clock cycle | tcyul |  | - | - | 30.518 | - | $\mu \mathrm{s}$ | When using external clock |
| Input clock pulse width | - |  | Pwh/toyll <br> PwL/tcyll | 45 | - | 55 | \% | When using external clock |
| Input clock rise time and fall time | $\begin{aligned} & \text { tcF } \\ & \text { tcr } \end{aligned}$ |  | - | - | - | 200 | ns | When using external clock |


(3) Conditions of PLL
$\left(\mathrm{V} \mathrm{cc}=\mathrm{AV} \mathrm{cc}=2.7 \mathrm{~V}\right.$ to 3.6 V , V ss $=\mathrm{AV} \mathrm{ss}=0 \mathrm{~V}, \mathrm{Ta}=-40^{\circ} \mathrm{C}$ to $\left.+85^{\circ} \mathrm{C}\right)$

| Parameter | Symbol | Conditions | Value |  |  | Remarks |  |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Typ | Max |  |  |  |
| PLL oscillation <br> stabilization wait time <br> (LOCK UP time) | tLock | - | 600 | - | - | $\mu \mathrm{s}$ | Time from when the PLL <br> starts operating until the <br> oscillation stabilizes |
| PLL input clock <br> frequency | fPLL | - | 4 | - | 24 | MHz |  |
| PLL multiple rate | - | - | 2 | - | 15 | Multiplied <br> by |  |
| PLL macro oscillation <br> clock frequency | fPLLo | - | 30 | - | 60 | MHz |  |

(4) Regulator Voltage Stabilization Wait Time
$\left(\mathrm{V} \mathrm{Cc}=\mathrm{AV} \mathrm{cc}=2.7 \mathrm{~V}\right.$ to $3.6 \mathrm{~V}, \mathrm{~V}_{\mathrm{ss}}=\mathrm{AV} \mathrm{ss}=0 \mathrm{~V}, \mathrm{Ta}=-40^{\circ} \mathrm{C}$ to $\left.+85^{\circ} \mathrm{C}\right)$

| Parameter | Symbol | Conditions | Value |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max |  |  |
| Regulator voltage stabilization wait time | treg | - | 50 | - | $\mu \mathrm{s}$ | Time taken for the regulator voltage to stabilize |

Note : This is the time from when the external power supply stabilizes (after reaching 2.7 V).

## MB91625 Series

(7) Synchronous serial (CSIO) timing
$\left(\mathrm{Vcc}=\mathrm{AV} \mathrm{cc}=2.7 \mathrm{~V}\right.$ to 3.6 V , $\mathrm{Vss}=\mathrm{AV} \mathrm{ss}=0 \mathrm{~V}, \mathrm{Ta}=-40^{\circ} \mathrm{C}$ to $\left.+85^{\circ} \mathrm{C}\right)$

- Synchronous serial (SPI $=0, \operatorname{SCINV}=0)$

| Parameter | Symbol | Pin name | Conditions | Value |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |
| Serial clock cycle time | tscyc | SCKn | Internal shift clock operation | 4tcycp | - | ns |
| SCK $\downarrow \rightarrow$ SOUT delay time | tslovi | $\begin{aligned} & \hline \text { SCKn } \\ & \text { SOUTn } \end{aligned}$ |  | - 30 | $+30$ | ns |
| SIN $\rightarrow$ SCK $\uparrow$ setup time | tivshi | SCKn SINn |  | 45 | - | ns |
| SCK $\uparrow \rightarrow$ SIN hold time | tshixI | SCKn SINn |  | 0 | - | ns |
| Serial clock "L" pulse width | tsLsh | SCKn | External shift clock operation | 2tcycp - 10 | - | ns |
| Serial clock "H" pulse width | tshsL | SCKn |  | tcycp + 10 | - | ns |
| SCK $\downarrow \rightarrow$ SOUT delay time | tslove | $\begin{aligned} & \text { SCKn } \\ & \text { SOUTn } \end{aligned}$ |  | - | 40 | ns |
| SIN $\rightarrow$ SCK $\uparrow$ setup time | tivshe | SCKn SINn |  | 15 | - | ns |
| SCK $\uparrow \rightarrow$ SIN hold time | tshixe | SCKn SINn |  | 20 | - | ns |
| SCK fall time | $\mathrm{t}_{\mathrm{F}}$ | SCKn | - | - | 5 | ns |
| SCK rise time | tR | SCKn | - | - | 5 | ns |

Notes: • The above standards apply to CLK synchronous mode.

- tcrcp indicates the peripheral clock cycle time.
- When the external load capacitance $C=50 \mathrm{pF}$.



## MB91625 Series



- Synchronous serial (SPI = 0, SCINV = 1)

| Parameter | Symbol | Pin name | Conditions | Value |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |
| Serial clock cycle time | tscyc | SCKn | Internal shift clock operation | 4tcycp | - | ns |
| SCK $\uparrow \rightarrow$ SOUT delay time | tshovi | SCKn SOUTn |  | - 30 | + 30 | ns |
| SIN $\rightarrow$ SCK $\downarrow$ setup time | tivsLı | sCKn SINn |  | 45 | - | ns |
| SCK $\downarrow \rightarrow$ SIN hold time | tsLIxI | SCKn SINn |  | 0 | - | ns |
| Serial clock "L" pulse width | tsısh | SCKn | External shift clock operation | 2tcycp - 10 | - | ns |
| Serial clock "H" pulse width | tshsL | SCKn |  | tCYCP + 10 | - | ns |
| SCK $\uparrow \rightarrow$ SOUT delay time | tshove | SCKn SOUTn |  | - | 40 | ns |
| SIN $\rightarrow$ SCK $\downarrow$ setup time | tivsle | SCKn SINn |  | 15 | - | ns |
| SCK $\downarrow \rightarrow$ SIN hold time | tstixe | SCKn SINn |  | 20 | - | ns |
| SCK fall time | $\mathrm{t}_{\mathrm{F}}$ | SCKn |  | - | 5 | ns |
| SCK rise time | tR | SCKn |  | - | 5 | ns |

Notes: • The above standards apply to CLK synchronous mode.

- tcycp indicates the peripheral clock cycle time.
- When the external load capacitance $C=50 \mathrm{pF}$.

$M S$ bit $=1$


## MB91625 Series

- Synchronous serial (SPI = 1,SCINV =0)

| Parameter | Symbol | Pin name | Conditions | Value |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |
| Serial clock cycle time | tscyc | SCKn | Internal shift clock operation | 4tcycp | - | ns |
| SCK $\uparrow \rightarrow$ SOUT delay time | tshovi | SCKn SOUTn |  | -30 | + 30 | ns |
| SIN $\rightarrow$ SCK $\downarrow$ setup time | tıssu | $\begin{aligned} & \hline \text { SCKn } \\ & \text { SINn } \end{aligned}$ |  | 45 | - | ns |
| SCK $\downarrow \rightarrow$ SIN hold time | tsuxı | $\begin{aligned} & \hline \text { SCKn } \\ & \text { SINn } \end{aligned}$ |  | 0 | - | ns |
| SOUT $\rightarrow$ SCK $\downarrow$ delay time | tsovıı | $\begin{aligned} & \hline \text { SCKn } \\ & \text { SOUTn } \end{aligned}$ |  | 2tcycp - 30 | - | ns |
| Serial clock "L" pulse width | tsısh | SCKn | External shift clock operation | 2tcycp - 10 | - | ns |
| Serial clock "H" pulse width | tshsL | SCKn |  | tcycp + 10 | - | ns |
| SCK $\uparrow \rightarrow$ SOUT delay time | tshove | SCKn SOUTn |  | - | 40 | ns |
| SIN $\rightarrow$ SCK $\downarrow$ setup time | tivsLe | $\begin{aligned} & \hline \text { SCKn } \\ & \text { SINn } \end{aligned}$ |  | 15 | - | ns |
| SCK $\downarrow \rightarrow$ SIN hold time | tslıe | $\begin{aligned} & \text { SCKn } \\ & \text { SINn } \end{aligned}$ |  | 20 | - | ns |
| SCK fall time | tF | SCKn |  | - | 5 | ns |
| SCK rise time | tR | SCKn |  | - | 5 | ns |

Notes: - The above standards apply to CLK synchronous mode.

- tcycp indicates the peripheral clock cycle time.
- When the external load capacitance $C=50 \mathrm{pF}$.

$M S$ bit $=0$


## MB91625 Series



- Synchronous serial (SPI = 1, SCINV = 1)

| Parameter | $\begin{aligned} & \text { Sym- } \\ & \text { bol } \end{aligned}$ | Pin name | Conditions | Value |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |
| Serial clock cycle time | tscrc | SCKn | Internal shift clock operation | 4tcycp | - | ns |
| SCK $\downarrow \rightarrow$ SOUT delay time | tsovi | $\begin{aligned} & \text { SCKn } \\ & \text { SOUTn } \end{aligned}$ |  | -30 | +30 | ns |
| SIN $\rightarrow$ SCK $\uparrow$ setup time | tivsFI | $\begin{aligned} & \text { SCKn } \\ & \text { SINn } \end{aligned}$ |  | 45 | - | ns |
| SCK $\uparrow \rightarrow$ SIN hold time | tshixI | $\begin{aligned} & \text { SCKn } \\ & \text { SINn } \end{aligned}$ |  | 0 | - | ns |
| SOUT $\rightarrow$ SCK $\uparrow$ delay time | tsover | $\begin{aligned} & \text { SCKn } \\ & \text { SOUTn } \end{aligned}$ |  | 2tcycp - 30 | - | ns |
| Serial clock "L" pulse width | tstsh | SCKn | External shift clock operation | 2tcycp - 10 | - | ns |
| Serial clock "H" pulse width | tsHSL | SCKn |  | tcycp + 10 | - | ns |
| SCK $\downarrow \rightarrow$ SOUT delay time | tslove | $\begin{aligned} & \text { SCKn } \\ & \text { SOUTn } \end{aligned}$ |  | - | 40 | ns |
| SIN $\rightarrow$ SCK $\uparrow$ setup time | tivshe | $\begin{aligned} & \text { SCKn } \\ & \text { SINn } \end{aligned}$ |  | 15 | - | ns |
| SCK $\uparrow \rightarrow$ SIN hold time | tshixe | $\begin{aligned} & \text { SCKn } \\ & \text { SINn } \end{aligned}$ |  | 20 | - | ns |
| SCK fall time | tF | SCKn |  | - | 5 | ns |
| SCK rise time | tr | SCKn |  | - | 5 | ns |

Notes: - The above standards apply to CLK synchronous mode.

- tcycp indicates the peripheral clock cycle time.
- When the external load capacitance $C=50 \mathrm{pF}$.


## MB91625 Series



- External clock (EXT = 1) : asynchronous only

| Parameter | Symbol | Conditions | Value |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  | Min | Max |  |
| Serial clock "L" pulse width | tsısh | $C L=50 \mathrm{pF}$ | tcycp + 10 | - | ns |
| Serial clock "H" pulse width | tshsL |  | tcycp + 10 | - | ns |
| SCK fall time | tF |  | - | 5 | ns |
| SCK rise time | tR |  | - | 5 | ns |

SCK


## MB91625 Series

(8) Free-run Timer Clock, Reload Timer Event Input, Up/down Counter Input, Input Capture Input, Interrupt Input Timing

$$
\left(\mathrm{Vcc}=\mathrm{AV} \mathrm{cc}=2.7 \mathrm{~V} \text { to } 3.6 \mathrm{~V}, \mathrm{~V} \mathrm{ss}=\mathrm{AV} \mathrm{ss}=0 \mathrm{~V}, \mathrm{Ta}=-40^{\circ} \mathrm{C} \text { to }+85^{\circ} \mathrm{C}\right)
$$

| Parameter | Symbol | Pin name | Conditions | Value |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max |  |  |
| Input pulse width | tтwh ttiwn | $\begin{gathered} \hline \text { FRCKn } \\ \text { TMIn } \\ \text { INn } \\ \text { AINn } \\ \text { BINn } \\ \text { ZINn } \end{gathered}$ | - | 2 tcycp | - | ns | *1 |
|  |  | INTn | - | 3 toycp | - | ns | *1 |
|  |  |  | - | 1.0 | - | $\mu \mathrm{s}$ | *2 |

*1: tcycp indicates peripheral clock cycle time, except when in stop mode, in main timer mode and in watch mode.
*2 : When in stop mode, in main timer mode, or in watch mode.

(9) A/D Converter Trigger Input Timing
$\left(\mathrm{V} \mathrm{cc}=\mathrm{AV} \mathrm{cc}=2.7 \mathrm{~V}\right.$ to 3.6 V , $\mathrm{V} \mathrm{ss}=\mathrm{AV} \mathrm{ss}=0 \mathrm{~V}, \mathrm{Ta}=-40^{\circ} \mathrm{C}$ to $\left.+85^{\circ} \mathrm{C}\right)$

| Parameter | Symbol | Pin name | Condi- <br> tions | Value |  | Unit | Remarks |
| :--- | :---: | :---: | :---: | :---: | :---: | :---: | :--- |
| A/D converter trigger <br> input |  | ADTRGn |  | 2 tcycp | - |  | * |

* : tcycp indicates peripheral clock cycle time.



## MB91625 Series

(10) ${ }^{12} \mathrm{C}$ Timing
$\left(\mathrm{V} \mathrm{cc}=\mathrm{AV} \mathrm{cc}=2.7 \mathrm{~V}\right.$ to 3.6 V , V ss $=\mathrm{AV} \mathrm{ss}=0 \mathrm{~V}, \mathrm{Ta}=-40^{\circ} \mathrm{C}$ to $\left.+85^{\circ} \mathrm{C}\right)$

| Parameter | Symbol | Pin name | Condition | Typical mode |  | High-speed mode |  | Unit |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  |  |  | Min | Max | Min | Max |  |
| SCL clock frequency | fscl | $\begin{aligned} & \hline \text { SCKn } \\ & \text { (SCLn) } \end{aligned}$ | $\begin{gathered} \mathrm{C}_{\mathrm{L}}=50 \mathrm{pF} \\ \mathrm{R}=(\mathrm{Vp} / \mathrm{loL})^{\star_{1}} \end{gathered}$ | 0 | 100 | 0 | 400 | kHz |
| "(Repeated) START condition" hold time SDA $\downarrow \rightarrow$ SCL $\downarrow$ | thosta | SOUTn (SDAn) SCKn (SCLn) |  | 4.0 | - | 0.6 | - | $\mu \mathrm{S}$ |
| SCL clock "L" width | tıow | $\begin{aligned} & \hline \text { SCKn } \\ & \text { (SCLn) } \end{aligned}$ |  | 4.7 | - | 1.3 | - | $\mu \mathrm{s}$ |
| SCL clock "H" width | thigh | $\begin{aligned} & \text { SCKn } \\ & \text { (SCLn) } \end{aligned}$ |  | 4.0 | - | 0.6 | - | $\mu \mathrm{s}$ |
| "Repeated START condition" setup time SCL $\uparrow \rightarrow$ SDA $\downarrow$ | tsusta | $\begin{aligned} & \text { SCKn } \\ & \text { (SCLn) } \end{aligned}$ |  | 4.7 | - | 0.6 | - | $\mu \mathrm{s}$ |
| Data hold time SCL $\downarrow \rightarrow$ SDA $\downarrow \uparrow$ | thidat | SOUTn (SDAn) SCKn (SCLn) |  | 0 | $3.45{ }^{* 2}$ | 0 | 0.9*3 | $\mu \mathrm{s}$ |
| Data setup time SDA $\downarrow \uparrow \rightarrow$ SCL $\uparrow$ | tsudat | SOUTn (SDAn) SCKn (SCLn) |  | 250 | - | 100 | - | ns |
| "STOP condition" setup time SCL $\uparrow \rightarrow$ SDA $\uparrow$ | tsusto | SOUTn (SDAn) SCKn (SCLn) |  | 4.0 | - | 0.6 | - | $\mu \mathrm{s}$ |
| Bus free time between "STOP condition" and "START condition" | tbuf | - |  | 4.7 | - | 1.3 | - | $\mu \mathrm{s}$ |
| Noise filter | tsp | - | - | 2tcycp*4 | - | $2 \mathrm{tcycp}{ }^{* 4}$ | - | ns |

*1: R and C represent the pull-up resistance and load capacitance of the SCL and SDA lines, respectively. Vp indicates the power supply voltage of the pull-up resistance and loL indicates Vol guaranteed current.
*2 : The maximum thdдat must satisfy that it doesn't extend at least "L" period (tow) of device's SCL signal.
*3: A high-speed mode $I^{2} \mathrm{C}$ bus device can be used on a standard mode $I^{2} \mathrm{C}$ bus system as long as the device satisfies the requirement of "tsudat $\geq 250 \mathrm{~ns}$ ".
*4 : tcycp is the peripheral clock cycle time. To use $\mathrm{I}^{2} \mathrm{C}$, set the peripheral bus clock at 8 MHz or more.

## MB91625 Series



## MB91625 Series

## 5. Electrical Characteristics for the A/D Converter

| Parameter | Pin name | Value |  |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |
| Resolution | - | - | - | 10 | bit |  |
| Total error | - | - 5.0 | - | + 5.0 | LSB |  |
| Linearity error | - | -3.5 | - | + 3.5 | LSB |  |
| Differential linearity error | - | -3 | - | + 3 | LSB |  |
| Zero transition voltage | $\begin{gathered} \text { ANO } \\ \text { to } \\ \text { AN15 } \end{gathered}$ | -1.5 | + 0.5 | +4 | LSB | $\begin{aligned} & \mathrm{AV} \mathrm{cc}=3.3 \mathrm{~V}, \\ & \mathrm{AVRH}=3.3 \mathrm{~V} \end{aligned}$ |
| Full transition voltage | $\begin{gathered} \text { AN0 } \\ \text { to } \\ \text { AN15 } \end{gathered}$ | AVRH - 4 | AVRH - 1.5 | AVRH + 0.5 | LSB |  |
| Compare time | - | $0.72^{* 3}$ | - | - | $\mu \mathrm{s}$ | PCLK $=33 \mathrm{MHz}$ |
| Conversion time | - | $1.2{ }^{* 1}$ | - | - | $\mu \mathrm{s}$ | PCLK $=33 \mathrm{MHz}$ |
| Power supply current (analog + digital) | AVcc | - | - | 3.5 | mA | When operating A/D <br> (with D/A stopped) |
|  |  | - | - | 11 | $\mu \mathrm{A}$ | At power-down*2 |
| Reference power supply current (between AVRH and AVss) | AVRH | - | - | 0.6 | mA | When operating A/D $\mathrm{AVRH}=3.0 \mathrm{~V}$ |
|  |  | - | - | 5 | $\mu \mathrm{A}$ | At power-down*2 |
| Analog input capacitance | - | - | - | 8.5 | pF |  |
| Interchannel disparity | - | - | - | 4 | LSB |  |
| Analog port input current | ANO to AN15 | - | - | 10 | $\mu \mathrm{A}$ |  |
| Analog input voltage | ANO to AN15 | AVss | - | AVRH | V |  |
| Reference voltage | AVRH | AVss | - | AVcc | V |  |

*1: It depends on the actual external load and the clock cycle supplied to peripheral resources. Make sure to satisfy PCLK cycle $\times 4$ or over + below (Equation 1). The condition of minimum conversion time is the value when PCLK $=33 \mathrm{MHz}$, sampling time: $0.424 \mu \mathrm{~s}$, external impedance: $1.4 \mathrm{k} \Omega$ or below, compare time: $0.72 \mu \mathrm{~s}$.
*2 : The current when the CPU is in stop mode and the A/D converter is not operating.
*3 : Compare time $=\{(C T+1) \times 10+4\} \times$ peripheral clock (PCLK) period. (CT indicates compare time setting bits.) The condition of the minimum compare time is when $\mathrm{CT}=1$ and $\mathrm{PCLK}=33 \mathrm{MHz}$.
(Continued)

## MB91625 Series

(Continued)


The output impedance of the external circuit connected to the analog input affects the sampling time of the A/D converter. Design the output impedance of the output circuit such that the required sampling time is less than the value of Ts calculated from the following equation.
(Equation1) Ts $=($ Rin + Rext $) \times \operatorname{Cin} \times 8$
Ts : Sampling time
Rin : Input resistance of $A / D=5.3 \mathrm{k} \Omega$
Cin : Input capacitance of $\mathrm{A} / \mathrm{D}=8.5 \mathrm{pF}$
Rext : Output impedance of external circuit
If the sampling time is set as 600 ns ,
$600 \mathrm{~ns} \geq(5.3 \mathrm{k} \Omega+$ Rext $) \times 8.5 \mathrm{pF} \times 8$
$\therefore$ Rext $\leq 3.5 \mathrm{k} \Omega$
And the impedance of the external circuit therefore needs to be $3.5 \mathrm{k} \Omega$ or less.

## MB91625 Series

(Continued)


## MB91625 Series

## 6. Electrical Characteristics for the D/A Converter

$\left(\mathrm{Vcc}=\mathrm{AV} \mathrm{cc}=2.7 \mathrm{~V}\right.$ to 3.6 V , $\mathrm{Vss}=\mathrm{AV} \mathrm{ss}=0 \mathrm{~V}, \mathrm{Ta}=-40^{\circ} \mathrm{C}$ to $\left.+85^{\circ} \mathrm{C}\right)$

| Parameter | Pin name | Value |  |  | Unit | Remarks |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | Min | Typ | Max |  |  |
| Resolution | - | - | - | 8 | bit |  |
| Linearity error | - | -2.0 | - | +2.0 | LSB | When the output is unloaded |
| Differential linearity error | - | - 1.0 | - | + 1.0 | LSB | When the output is unloaded |
| Conversion time | - | - | 0.6 | - | $\mu \mathrm{s}$ | When load capacitance $\left(C_{L}\right)=20 \mathrm{pF}$ |
|  | - | - | 3.0 | - | $\mu \mathrm{s}$ | When load capacitance $(\mathrm{CL})=100 \mathrm{pF}$ |
| Analog output impedance | DA0, DA1 | 3.19 | 3.51 | 5.85 | k $\Omega$ |  |
| Analog current | AVcc | - | 300 | - | $\mu \mathrm{A}$ | $10 \mu \mathrm{~s}$ conversion, when the output is unloaded (When 2 channels operating, A/D stopped) |
|  |  | - | - | 3600* | $\mu \mathrm{A}$ | When the input digital code is fixed at 7 Ан or 85 н (When 2 channels operating, $\mathrm{A} / \mathrm{D}$ stopped) |
|  |  | - | - | 11 | $\mu \mathrm{A}$ | At power-down (When A/D stopped) |

*: The current consumption of the D/A converter varies with input digital code. The standard value indicates the current consumed when the digital code that maximizes the current consumption is input.

## MB91625 Series

## 7. Flash Memory Write/Erase Characteristics

$$
\left(\mathrm{Vcc}=3.3 \mathrm{~V}, \mathrm{Ta}=+25^{\circ} \mathrm{C}\right)
$$

| Parameter | Value |  |  | Unit | Remarks |  |
| :--- | :---: | :---: | :---: | :---: | :--- | :---: |
|  | Min | Typ | Max |  |  |  |
| Sector erase time | - | 0.9 | 3.6 | s | Excludes write time prior to internal erase |  |
| Half word (16 bits) write <br> time | - | 23 | 370 | $\mu \mathrm{~s}$ | Not including system-level overhead time. |  |
| Chip erase time ${ }^{\star 1}$ | - | 7.2 | 28.8 | s | Excludes write time prior to internal erase <br> (When equipped with 512 Kbytes$)$ |  |
| Erase/write cycles | 10000 | - | - | cycle | Average $\mathrm{Ta} \leq+85^{\circ} \mathrm{C}$ |  |
| Flash memory <br> data hold time | $10^{\star 2}$ | - | - | year | Average $\mathrm{Ta} \leq+85^{\circ} \mathrm{C}$ |  |

*1: The chip erase time is the sector erase time multiplied across all sectors.
*2: This value comes from the technology qualification (using Arrhenius equation to translate high temperature measurements into normalized value at $+85^{\circ} \mathrm{C}$ ).

## MB91625 Series

## PACKAGE DIMENSION




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